OPERATION AND SERVICE MANUAL

Model 9642

PACE MICROPROCESSOR SUBSYSTEM
APPENDIX TO THE VM-4A SYSTEM MANUAL
Preliminary Issue

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Model 9642

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APPENDIX TO THE VM-4A SYSTEM
MANUAL

Preliminary Issue

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SECTION 1
GENERAL DESCRIPTION

1.1 INTRODUCTION

This appendix to the VM-4A Operation and Maintenance manual describes the Model 9642 Instrument Controller (PACE microprocessor subsystem) manufactured by Instrumentation Technology Systems, Northridge, California.

The PACE microprocessor (uP) subsystem is designed to integrate with the VM-4A Attenuator and Signal Generator Calibrator System, and provide the means to communicate, compute, and control functions of operation interaction. For convenience, the PACE uP subsystem will hereinafter be referred to as the controller.

1.2 APPLICABLE DOCUMENTS

PACE Technical Description, National Semiconductor Corporation Publication Number 4200078B.

PACE Logic Designers Guide to Programmed Equivalents to TTL functions, National Semiconductor Corporation Publication Number 420012X7 Preliminary, Order Number IPC-16A/927.

PACE Microprocessor Assembly Language Programming Manual, National Semiconductor Corporation Publication Number 4200130A, Order Number IPC-16S/969Y, January 1977.

PACE Users Manual, National Semiconductor Corporation Publication Number 4200068X, Order Number IPC-16P/968X, Preliminary.

PACE Users Manual Change Notice Number 2, 8 July 1975.

1.2 APPLICABLE DOCUMENTS (Continued)

IEEE Standard 488-1975 Digital Interface for Programmable Instrumentation.

EIA RS-232-C Standard Interface Between Data Terminal Equipment and Data Communication Equipment Employing Serial Binary Data Interchange, August 1969.

Hewlett-Packard 9825A Calculator Operating and Programming, Part Number 09825-90000, Microfiche Number 09825-99000.

Hewlett-Packard 9825A Calculator General I/O Programming, Part Number 09825-90024, Microfiche Number 09825-99024.

Hewlett-Packard 9825A Calculator Extended I/O Programming, Part Number 09825-90025, Microfiche Number 09825-99025.

1.3 CHARACTERISTICS

The controller contains the software instruction set located in 10K of read-only-memory (ROM). Management of the system is provided by a National Semiconductor PACE Microprocessor. Data interface requirements, as applied to the digital exchange of information for programmable instrumentation systems, conform to the specifications of the Institute of Electrical and Electronic Engineers (IEEE) as set forth in standard STD-488.

1.4 MAJOR ASSEMBLIES

The major elements of the controller are contained on seven printed circuit cards which interface with a motherboard assembly. Table 1-1 lists the circuit card names, reference designations, Weinschel and ITS part numbers.

1.5 FUNCTIONAL DESCRIPTION

The following is a brief functional description of each circuit card; the data interface between cards is shown in Figure 1-1. (Refer to Section IV, Theory of Operation for a more detailed description of each card.)

1.5.1 PACE/ROM Card

The PACE/ROM card, located in card slot 1A9A1, is the central processing unit (CPU) for the Controller subsystem. This card provides the interface, via the subsystem data bus, which allows the exchange of data between all other elements of the subsystem, and the PACE microprocessor. The PACE/ROM card located in card slot 1A9A1, initiates and controls system timing with a 10.24 MHz crystal oscillator, and also divides the initial frequency to produce clock outputs of 6.25 us and 2.56 MHz. In addition to processing bus information and generating system timing, this card also contains the first 4K of read-only-memory (ROM) with the remaining 6K of ROM being assigned to the RAM/ROM RS232 card (paragraph 1.5.4).

TABLE 1-1

CIRCUIT CARD COMPLEMENT

Title and Reference Designation	Weinschel Part Number	ITS Part Number
PACE/ROM CARD 1A9A1	C190-287-2	1180111
RAM/ROM BUS BUFFER CARD 1A9A2	C190-287-3	1180160
FRONT PANEL CONTROLLER CARD 1A9A3	C190 284-4	1180103
RAM/ROM RS-232 CARD 1A9A4	D190-287-5	1180210
COMMAND/DATA CARD 1A9A5	C190-287-6	1180171
L.E.D. PARALLEL I/O CARD 1A9A7	C190-287 7	1180190
IEEE INTERFACE CARD 1A9A8	C190-287-8	1180141
MOTHERBOARD 1A9A9	B190-287-1	1170960

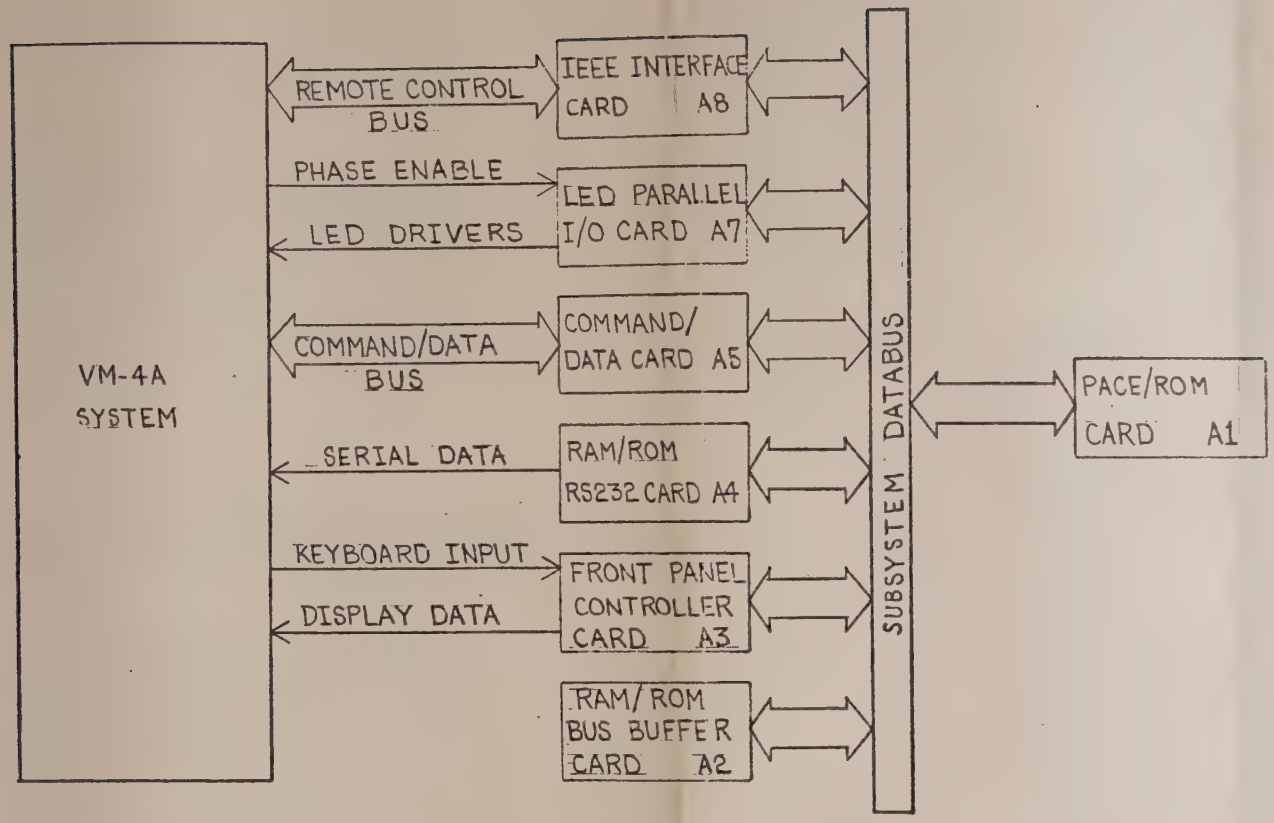


Figure 1-1,
PACE Microprocessor Subsystem,
Block Diagram

1.5.2 RAM/ROM Bus Buffer Card

The RAM/ROM bus buffer card, located in card slot 1A9A2, is dedicated to the control of the memory functions provided by the random-access-memory (RAM).

1.5.3 Front Panel Controller Card

The front panel controller card, located in card slot 1A9A3, accepts inputs from the VM-4A system keyboard. The keyboard information is coded and buffered, then sent out over the system data bus to interface with the CPU and other circuit cards contained within the controller. The front panel controller card also provides the necessary driver circuits required to produce visual messages. The messages, which are called from the appropriate software routines, are sent to the VM-4A system 40-character display.

1.5.4 RAM/ROM RS-232 Card

The RAM/ROM RS-232 card, located in card slot 1A9A4, performs two distinct functions. The first function is providing the remaining 6K of read-only-memory (ROM) to give the controller 10K of memory.

The second function is to provide a serial interface for the transfer of data over the RS-232-C line. Input processor information is applied to a universal asynchronous receiver transmitter (UART), and converted to serial data format for transfer to an external printer.

1.5.5 Command/Data Card

The command/data card, located in card slot 1A9A5, is the primary interface between the VM-4A system and the controller subsystem. The logic associated with the command/data bus maintains the proper communications protocol between the microprocessor and the instrument subsystems of the VM-4A system.

1.5.6. L.E.D. Parallel I/O Card

The L.E.D. parallel I/O card, located in card slot 1A9A7, drives the light emitting diodes (LEDs) on the front panel of the VM-4A system which indicate operating status. The phase enable signal input informs the microprocessor that the optional phase measurement device in the VM-4A system is installed.

1.5.7 IEEE Interface Card

The IEEE interface card, located in card slot 1A9A8, provides for remote control of the subsystem via an external input/output bus which conforms to IEEE standards. It enables the VM-4A system to control or be controlled, by any external peripheral device conforming to the IEEE standard for the exchange of data.

SECTION 11
INSTALLATION

2.1 INTRODUCTION

In this section, input power and environmental specification have been provided, as well as a general list of considerations which should be given attention prior to the application of power.

2.2 POWER REQUIREMENTS

The controller has been designed to operate from the voltage and current requirements listed in Table 2-1, using a recommended wire size of 14 gauge for input power.

2.3 MODULE INTERFACE

The motherboard assembly is structured so that the installed circuit cards have dedicated positions, with card slot A6 being designated as a spare and reserved for possible expansion. However, the system should not be configured with any of the existing circuit cards positioned in the spare location since certain functions are not common to card slot A6. Always remove or install circuit cards with power removed from the motherboard assembly. Figure 2-1 is the motherboard circuit card location chart.

2.4 SYSTEM INTERFACE

Connection to the controller is made from the bottom of the motherboard assembly, and has been designed to accommodate either wirewrap or connector coupling of signals to/from the VM-4A system.

TABLE 2-1

VOLTAGE SPECIFICATIONS

VOLTAGE	TOLERANCE	CURRENT
+5v	± 5%	6.5A
+12v	± 5%	0.025A
-12v	± 5%	0.225A

ENVIRONMENTAL REQUIREMENTS

Operating Temperature	0°C to + 50°C
Humidity	10% to 90% Relative, Non-Condensing
Barometric Pressure	Sea Level to 10,000 Feet

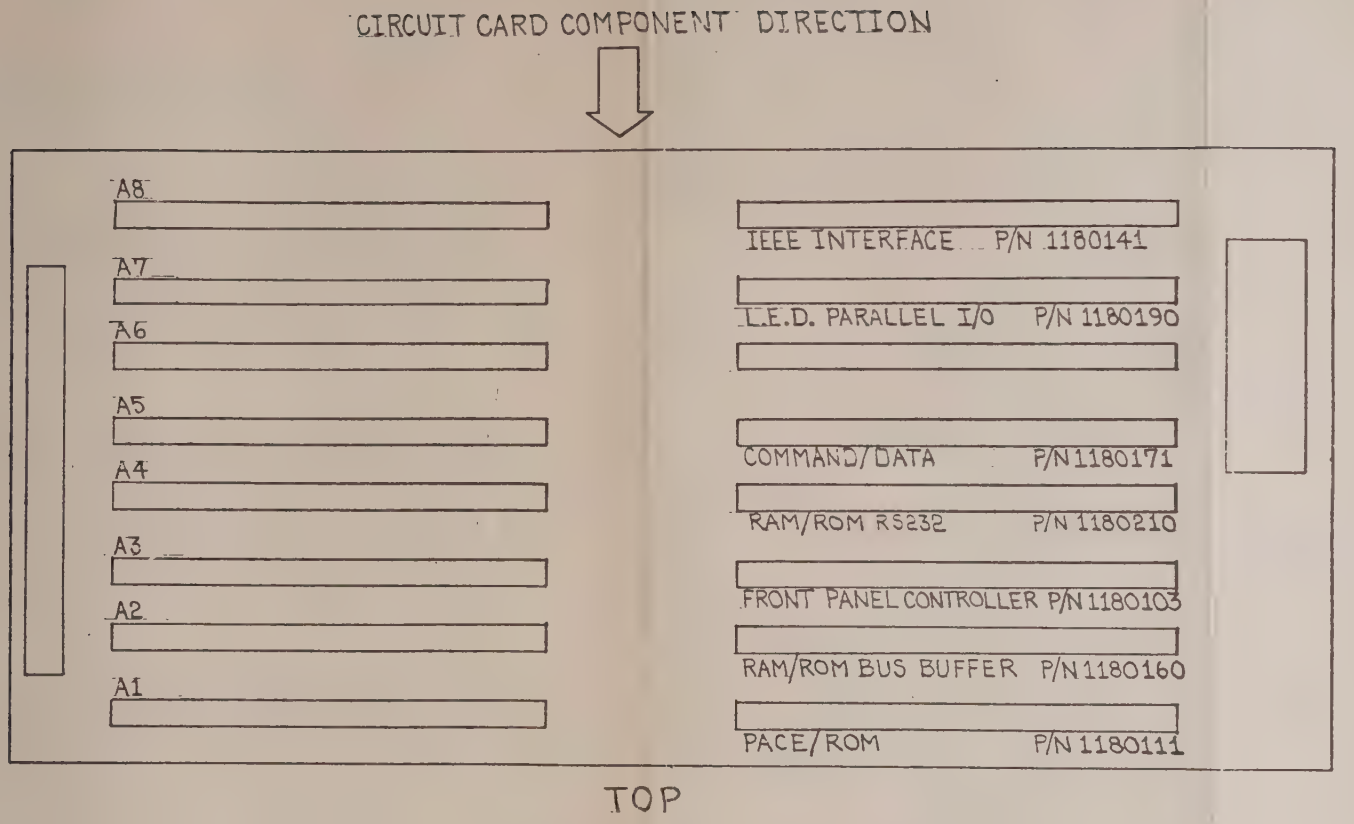


Figure 2-1,
PACE Motherboard,
Card Location Chart

SECTION III
OPERATION

3.1 INTRODUCTION

Microprocessor controlled functions are implemented by interaction between an operator, and the software instruction set contained in the read-only-memory (ROM) of the controller.

The operator must enter information, as to the measurement to be performed, and any parameters required to ensure reliable measured data. The software instruction set aids the operator, by providing cueing messages on the front panel display and indicating status and sequence by driving light emitting diodes (LEDs).

3.2 OPERATOR DIALOGUE

Manual data entry is provided by a keyboard encoder which is the complete keyboard interface system, and is capable of encoding up to 90 single-pole single-throw switch closures. The X input pins are numbered 1 thru 9, and are used to drive the key switch matrix. The Y input pins, numbered 1 thru 10, are the sense inputs and when activated with a given X input provide a tri-state output for utilization by the remaining controller circuitry.

The sequence of keyboard entry, as well as the definition of invalid entries, are not specified in this document. Refer to the VM-4A System Operation and Maintenance manual, Section III, for operating instructions.

3.3 OPERATOR INTERFACE

The controller and the software instruction set have been designed to follow specific operator action/reaction criteria, with certain functions taking priority over others.

The controller is set to its initial state by applying power to the unit. During this power-up sequence certain initial self tests are conducted which inform the operator of the possibility of error prior to moving to its initialization or wait-loop mode. The display will briefly indicate symbology during the power up sequence, however, no indication will be evident unless an error is discovered at which time the appropriate error message will be called from software.

3.4 CONTROLLER SELF-TEST

The self-test sequence is automatic, except for required operator action when performing the front panel key test. The VM-4A front panel uP SELF CHECK key allows initialization of the controller self-test sequence, and upon completion of the test must be pressed again to allow the software routine to more to the operating instruction set.

Table 3-2 outlines the controller self-test sequence, and Table 3-3 shows the error messages displayed during self-test failure modes.

TABLE 3-2

CONTROLLER SELF-TEST

TEST NUMBER	TEST TITLE	VM-4A DISPLAY
1	Visual Display Test	Entire display shows @ symbol
2	LED Driver Test	All LEDs light
3	CPU Test	Error message upon failure
4	RAM Test	Error message upon failure
5	ROM Test	Error message upon failure
6	Key Test	Key mnemonic and audible valid signal

TABLE 3-3

SELF-TEST ERROR MESSAGES

TEST TITLE	ERROR INDICATION
1. Visual Display Test	Any portion of display not lighted
2. LED Driver Test	Any LED not lighted
3. CPU Test	CPU ERROR
4. RAM Test	RAM ERROR A2 XXXX
5. ROM Test	ROM ERROR AX XXXX
6. Key Test	???

NOTE: XXXX RAM Error indication will list the location of any 1K group of bad memory.

XXXX ROM Error indication will list the circuit card location and any 2K block of bad memory.

SECTION IV

THEORY OF OPERATION

4.1 INTRODUCTION

This section of the manual presents hardware descriptions of each circuit card in the controller. Each description is supplemented with a block diagram of the circuit card assembly.

4.2 HARDWARE ORGANIZATION

The controller hardware consists of a motherboard assembly, and seven plug-in circuit cards which contain the necessary electronic devices required to perform the communication and computation functions.

4.3 PACE/ROM CARD 1A9A1 (Figures 4-1 and 5-1)

PACE/ROM card contains the microprocessor function of the controller. The microprocessor is a National Semiconductor PACE (CPU) module which communicates with memory and external devices over a 16-bit MOS bidirectional databus.

4.3.1 MOS/TTL Bus Conversion

The CPU MOS bus communicates with a TTL bus through bidirectional transceiver elements (BTE) which buffer the 16-bit, time multiplexed, address and data content of the two bidirectional data busses.

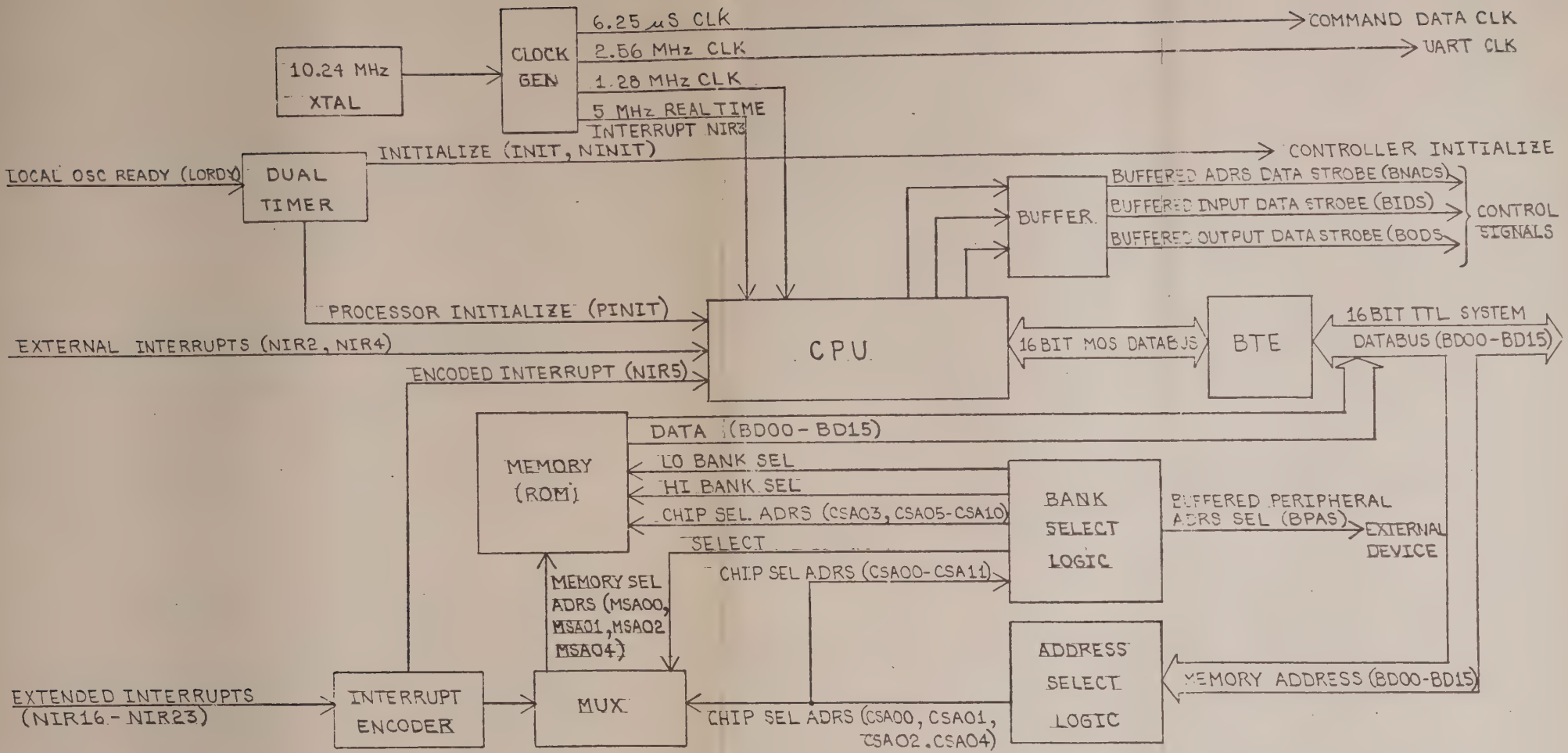


Figure 4-1.
PACE/ROM Card,
A9A1, Block Diagram

4.3.2 Memory Address

Under base page control, the first 128 memory address locations, which comprise the lower half of the base page, and the second 128 locations which are the upper half of the base page are addressable to allow mode selection of 128 locations in read-only-memory (ROM) or the selection of 128 address locations of random-access-memory (RAM).

Memory is divided into two 2048 word banks, with each bank containing four 2048 x 4 ROM modules. The low bank provides hexadecimal addresses 0000 thru 07FF and the high bank provides hexadecimal addresses 0800 thru 0FFF. The bank select logic determines if the address output from the CPU is in the low bank, high bank, or that of a peripheral device. It decodes the selected address, and provides the appropriate enable signal to memory or the peripheral device(s).

Address bits 0, 1, 2 and 4 of the selected address are sent to a multiplexer, as is the output of the interrupt encoder. The bank select logic also provides a select input to the multiplexer. When high bank is selected, the address bits are applied through the multiplexer to memory. When low bank is selected, the interrupt encoder outputs are applied to the memory. When interrupts occur on the encoder inputs, the multiplexer provides the means to modify address bits 00, 01, 02, and 04 so as to immediately point to those address locations in memory assigned to interrupts.

4.3.3 Interrupt Processing

Storage and priority encoding of external interrupts is provided, and the encoded signal is applied to the multiplexer. When any of the used interrupts are active, the logic supplies a signal to the CPU which then responds by supplying the vector address assigned to the interrupt.

The CPU accepts a real time interrupt from the clock generator on line NIR3 and external interrupts on lines NIR2, NIR4, and NIR5, with line NIR2 having the highest priority. To extend the interrupt capacity of the CPU, external interrupts on lines NIR16 thru NIR23 are applied to the interrupt encoder. They are decoded on a priority basis and applied to the CPU on line NIR5.

4.3.4 Timing

Timing reference for the CPU, the command/data card, and the UART on the RAM/ROM RS232 card is provided by a 10.24 MHz crystal-controlled clock generator. The clock generator provides a 6.25 us clock to the command data card, a 2.56 MHz clock to the UART, and a 1.28 MHz two-phase clock to the CPU. It also generates a 5 ms real time interrupt ot the CPU.

4.3.5 Initialization

The initialize timer is a dual timer module which provides initialization signals to the controller (NINIT, INIT) and CPU (PINIT). At power turn-on time, the inputs of both selections of the timer are held just above ground reference level of the local oscillator ready signal (LORDY) from the VM-4A system until all dc power supplies are producing outputs within the normal allowable range. When +5v becomes available for the operation of the timer, the NINIT and INIT outputs are switched high.

4.3.6 Control Signals

All data transfers between the CPU and external memories or devices take place over the 16-bit bidirectional databus and are synchronized by three buffered control signals (BNADS, BIDS, and BODS). All I/O transactions to the CPU consist of an address output interval, specifying a memory location or device, followed by a data transfer interval. The BNADS signal strobes the address data into an address storage element. The BIDS is the input data strobe and the BODS the output data strobe.

4.4 RAM/ROM BUS BUFFER CARD A2 (Figures 4-2 and 5-3)

The RAM/ROM bus buffer card contains three blocks of random-access-memory (RAM), and associated control functions. A block of memory consists of four 1024 x 4 RAM modules addressed by the CPU on PACE/ROM card A1 through the address storage and decode logic. The address storage and decode logic also generates a 2-bit binary RAM block address code.

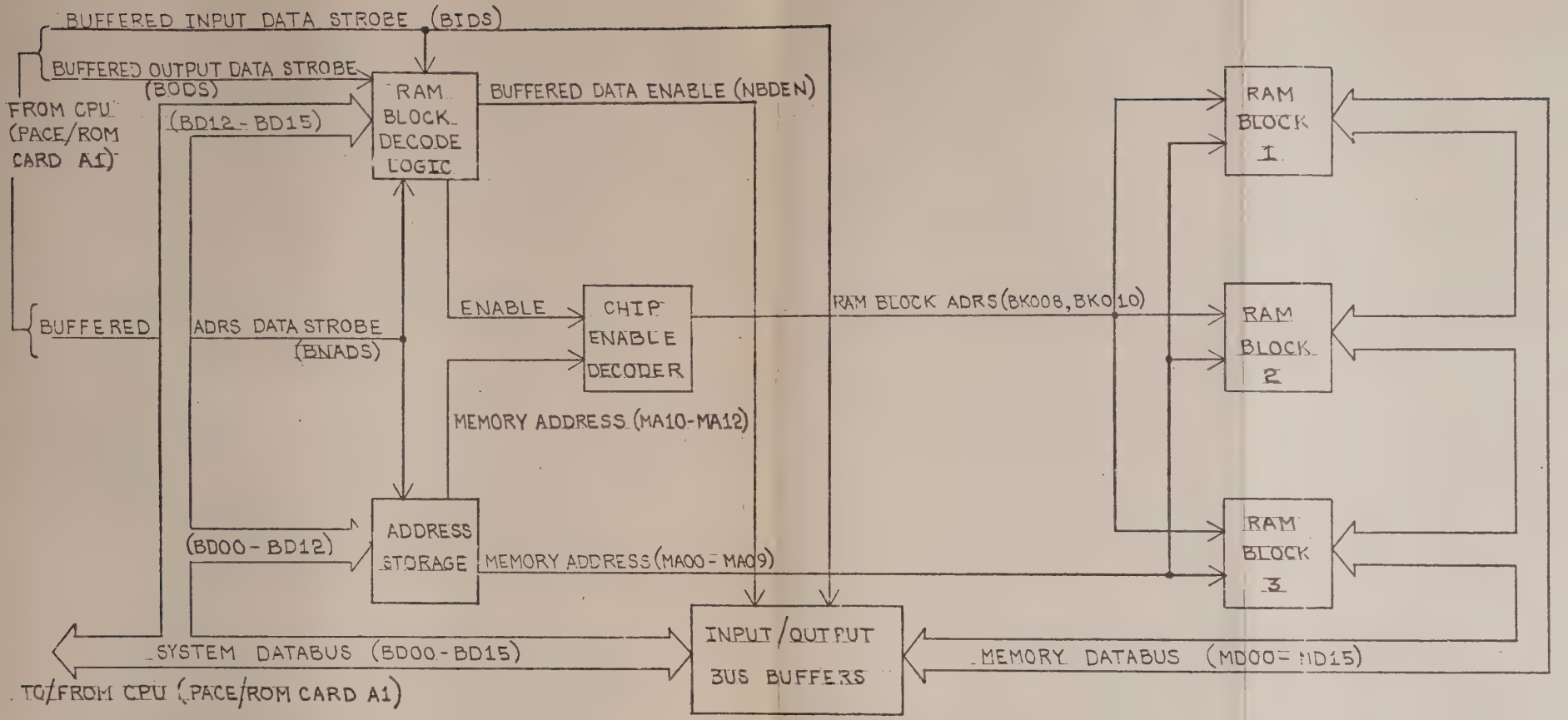


Figure 4-2,
RAM/ROM Bus Buffer Card,
A9A2, Block Diagram

4.4.1 Bus Buffers

The data outputs (MD00-MD15) of the three RAM blocks are connected to a common memory databus. The bus buffers provide bidirectional access between the memory databus lines and the system databus lines (BD00-BD15). The bus buffers which gate data from the CPU to the RAM blocks are enabled by a low BIDS control signal. The bus buffers which gate data from memory to the CPU are enabled by a low NBDEN signal from the address storage and decode logic.

4.4.2 Address Storage and Decode Logic

The address storage and decode logic consists of memory storage, RAM block decode logic, and a chip enable decoder. The memory storage provides storage capability for the 13 least significant bits (LSB) of memory address, the RAM block decode logic determines selection of the RAM block, and the chip enable decoder provides the RAM block address code. The address code consists of device enable and read/write enable signals.

The stored address is updated in response to the buffered address data strobe (BNADS) pulse. At this time the RAM block decode logic compares the preselected address field to the address bits on the system databus. If all compare bit values coincide, the decode logic compare output latches high, enabling the chip enable decoder. The chip enable decoder then outputs the RAM block address code.

4.5 FRONT PANEL CONTROLLER CARD A3 (Figures 4-3 and 5-5)

The front panel controller card provides the interface between the CPU and the VM-4A system front panel 40-character alphanumeric display and keyboard. The address storage and decode logic monitors for display and keyboard addresses (hexadecimal 8400 and 8402 respectively) during buffered address data strobe (BNADS) time and stores either of these addresses at the trailing edge of BNADS. When high, signals BPAS 1 and BD10 1 represent the two most significant hexadecimal digits. When these are received, high BD00 1 and BD01 1 signals identify address 8402 and low BD00 1 and BD01 1 signals identify address 8400.

4.5.1 Alphanumeric Display Logic

The alphanumeric display logic consists of recirculating storage registers, and provides storage for the forty characters of the alphanumeric display and generates the repetitive sequence required to regenerate the display. The alphanumeric display has two operating modes, the load-and-blanking mode and the recirculate mode. During each transmission of display character data from the CPU, a complete set of 40 characters is received. Each character is received on the BD00 1 thru BD05 1 lines and clocked into the recirculating storage registers in response to a DIND 0 pulse from the address storage and decode logic. (BODS pulses from the CPU are steered onto the DIND 0 line when the alphanumeric display address is stored in the address storage and decode logic.) The DIND 0 pulse associated with the first

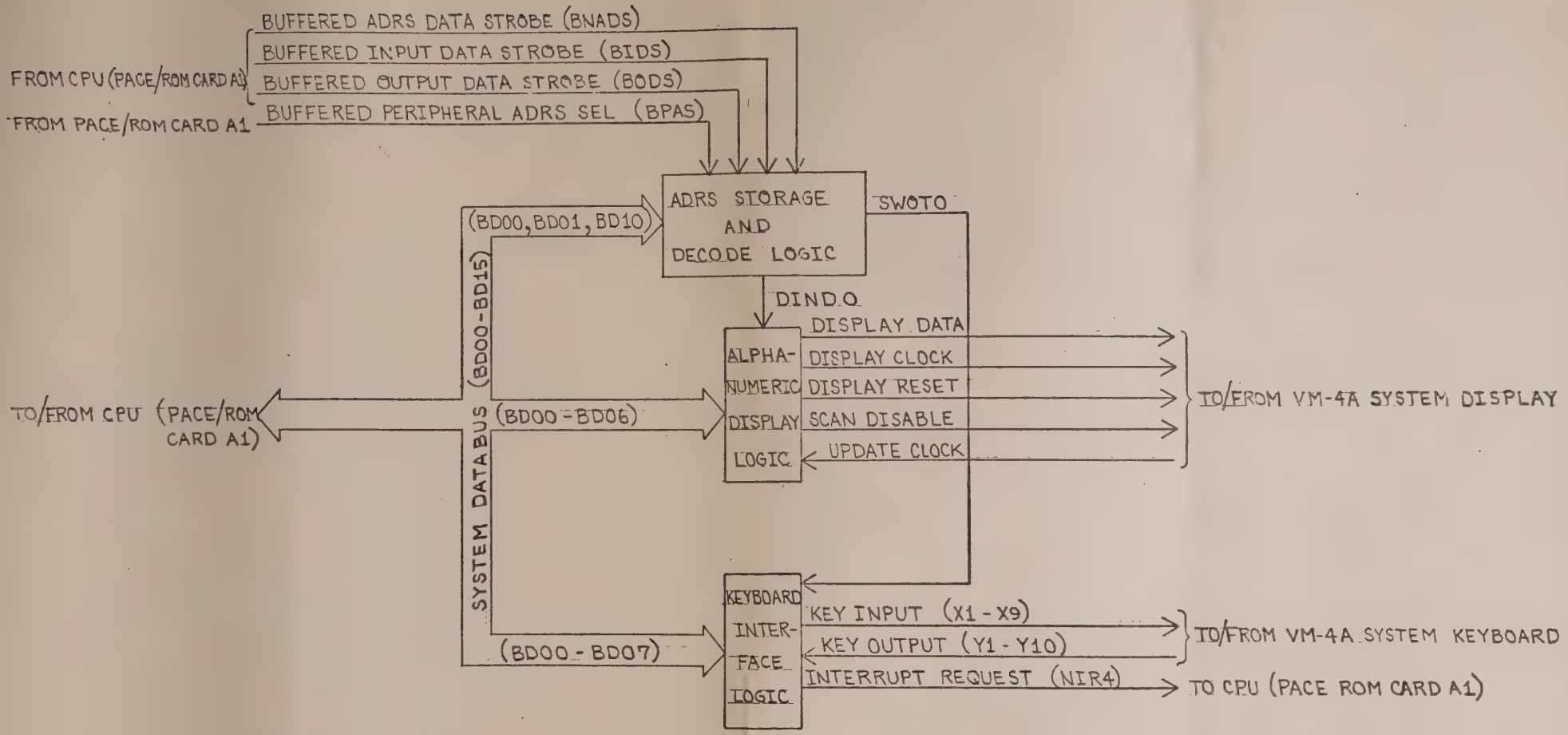


Figure 4-3,
Front Panel Controller Card,
A9A3, Block Diagram

4.5.1 Alphanumeric Display Logic (Continued)

received character switches the display logic into the load and blanking mode. When the 40th character is received from the CPU and stored, line BDO6 goes high, enabling the display logic to return to the recirculate mode.

In the recirculate mode, the display logic repetitively recirculates the characters held in storage and presents them in sequence to the display. The display converts the binary data specifying each character into a matrix of illuminated dots which provide the required character presentation. The timing of each regeneration cycle is controlled by four timing signals that pass between the display logic and the display. The DISPLAY RESET pulse from the display logic identifies the start of a regeneration cycle. The DISPLAY CLOCK signal from the display logic controls the display dot-matrix column timing. Seven columns are used for each character; the final two of these being blanked columns which provide the inter-character spacing. During every seventh DISPLAY CLOCK period, the display supplies an UPDATE CLOCK pulse to the display logic. These pulses are used to shift the stored data so as to present the next character to the display. Between the 40th character period and the start of the next scan cycle, the display logic supplies a SCAN DISABLE signal to the display. This controls blanking between successive regeneration cycles.

4.5.2 Keyboard Interface Logic

The keyboard interface logic consists of a keyboard encoder and associated logic. It provides the interface between the VM-4A system keyboard and the CPU. In response to actuation of a keyboard key, a character is encoded and stored and an interrupt request is initiated. The routine which services the interrput then reads the stored character and resets the interrupt flag.

The keyboard inputs are X1 thru X9, and outputs are Y1 thru Y10. The character encoding function is provided by the keyboard encoder module, with actuation of a particular key placing one X-output to one Y-input. The nine X-outputs and ten Y-inputs provide the capability of detecting the actuation of 90 keys. The particular code generated in response to any particular X-Y matrix pair depends upon the status of the SHIFT and CONTROL inputs. Thus, a total of 360 codes can be generated and stored, four for each of the 90 keys; however, in the VM-4A system, inputs are received from only 52 keys.

When a key is actuated, the keyboard interface logic converts the X-Y identifying code into an 8-bit binary code. It stores this code and initiates an NIR4 interrupt request to the CPU. The routine which services this interrupt reads the 8-bit character code from the keyboard interface logic. The transfer is implemented when the address storage and decode logic steers the buffered input data strobe (BIDS 1) pulse onto the SWOT 0 line as a result of having received the keyboard address during the

4.5.2 Keyboard Interface Logic (Continued)

preceding BNADS time. The SWOT 0 pulse is used to gate the stored 8-bit character code onto system databus lines BDOO 1 through BDO7 1 and to reset the NIR4 interrupt request.

4.6 RAM/ROM RS-232 CARD A4 (Figures 4-4 and 5-7)

The RAM/ROM RS232 card contains three blocks of read-only-memory (ROM), associated control functions, and serial interface logic which conforms to the EIA standard for RS-232 data. A block of memory consists of four 2K X 4 ROM modules addressed by the CPU on PACE/ROM card A1 through the address storage and decode logic. The address storage and decode logic also generates a 2-bit binary ROM block address code.

4.6.1 Bus Buffers

The data outputs (MD00-MD15) of the three ROM blocks are connected to a common memory databus. The bus buffers provide access between the memory databus lines and the system databus lines (BD00-BD15), and are enabled by a high BDEN signal from the address storage and decode logic.

4.6.2 Address Storage and Decode Logic

The address storage and decode logic consists of memory storage, ROM block decode logic, and a chip enable decoder. The memory storage provides storage capability for the 13 least significant bits (LSB) of memory address, the ROM block decode logic determines selection of the ROM block, and the chip enable decoder provides the ROM block address code. The address code consists of device enable and read enable signals.

The stored address is updated in response to the buffered address data strobe (BNADS) pulse. At this time the ROM block decode logic compares

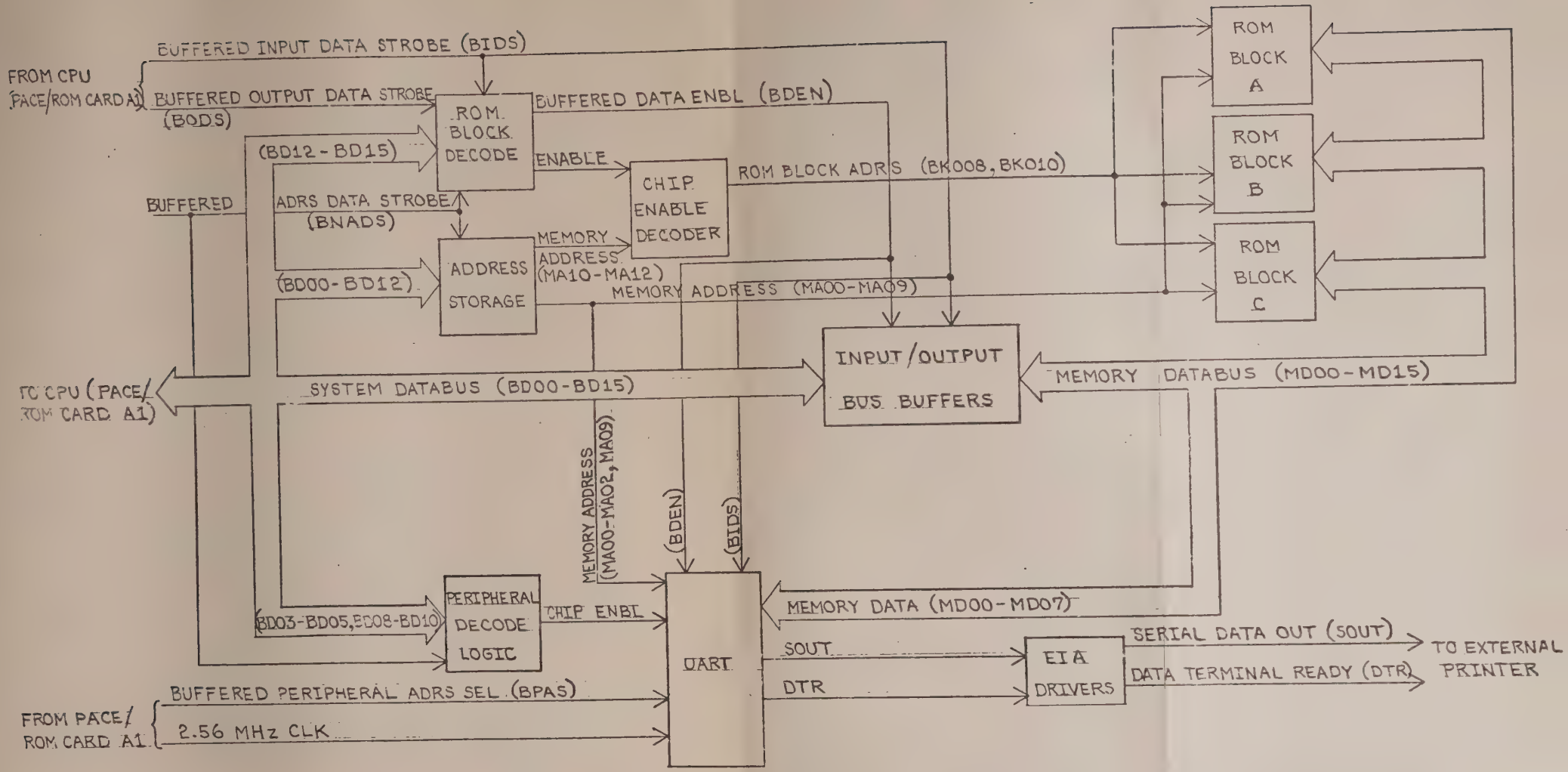


Figure 4-4,
RAM/ROM RS-232 Card
A9A4, Block Diagram

4.6.2 Address Storage and Decode Logic (Continued)

the preselected address field to the address bits on the system databus. If all compare bit values coincide, the decode logic compare output latches high, enabling the chip enable decoder. The chip enable decoder then outputs the ROM block address code.

4.6.3 Serial Interface Logic

The serial interface logic consists of peripheral decode logic, a UART, and EIA drivers. When addressed by the CPU, the UART performs parallel-to-serial conversion on data received from memory and transmits it at 1200 baud to an external printer.

During the BNADS time, the peripheral decode logic compares the preselected address field to the address bits on the system databus. When all compare bit values coincide, the decoder compare output latches high. If at this time, the buffered peripheral address select (BPAS) input is also high, and memory address bit MA11 is low, the UART is enabled. The UART reference clock is 2.56 MHz, and a 3-bit memory address code (MA00-MA02) selects the register into which the 8-bit memory data (MD00-MD07) input is to be entered. Data is entered during the time the buffered output data strobe (BODS) pulse is high. When the buffered input data strobe (BIDS) pulse is high, the CPU can read the status information or data in the selected UART register. When conversion is completed and the UART is ready to communicate, a low data terminal ready (DTR) signal is sent to the printer. The DTR signal

4.6.3 Serial Interface Logic (Continued)

and serial output are sent to the printer through EIA drivers which establish the proper RS-232-C levels.

4.7 COMMAND/DATA CARD A5 (Figures 4-5 and 5-9)

The command/data card functions as the primary interface between the VM-4A system and the controller. The card contains a 16-bit bidirectional latch, a 16-bit bidirectional buffer, input/output (I/O) select decode logic, address and strobe latches, strobe decode logic, and output buffers. Data and commands from the CPU is output to the applicable RF measurement devices, and data from the devices is input to the CPU. The CPU also provides the timing and control signals for these functions.

4.7.1 I/O Select Decode Logic

The CPU transfer address code (BD00, BD01, BD02, BD04, BD09) and buffered control signals (BNADS, BIDS, BODS), and the buffered peripheral address select (BPAS) signal are applied to the I/O select decode logic, which then generates the necessary signals to control the data transfer I/O functions of the command/data card.

4.7.2 Data Transfer I/O Control

The I/O functions of the 16-bit bidirectional latch are controlled by the clock (CLK), disable (DIS1), data output select (DOSEL0), and input enable (IENB0) signals from the I/O select decode logic.

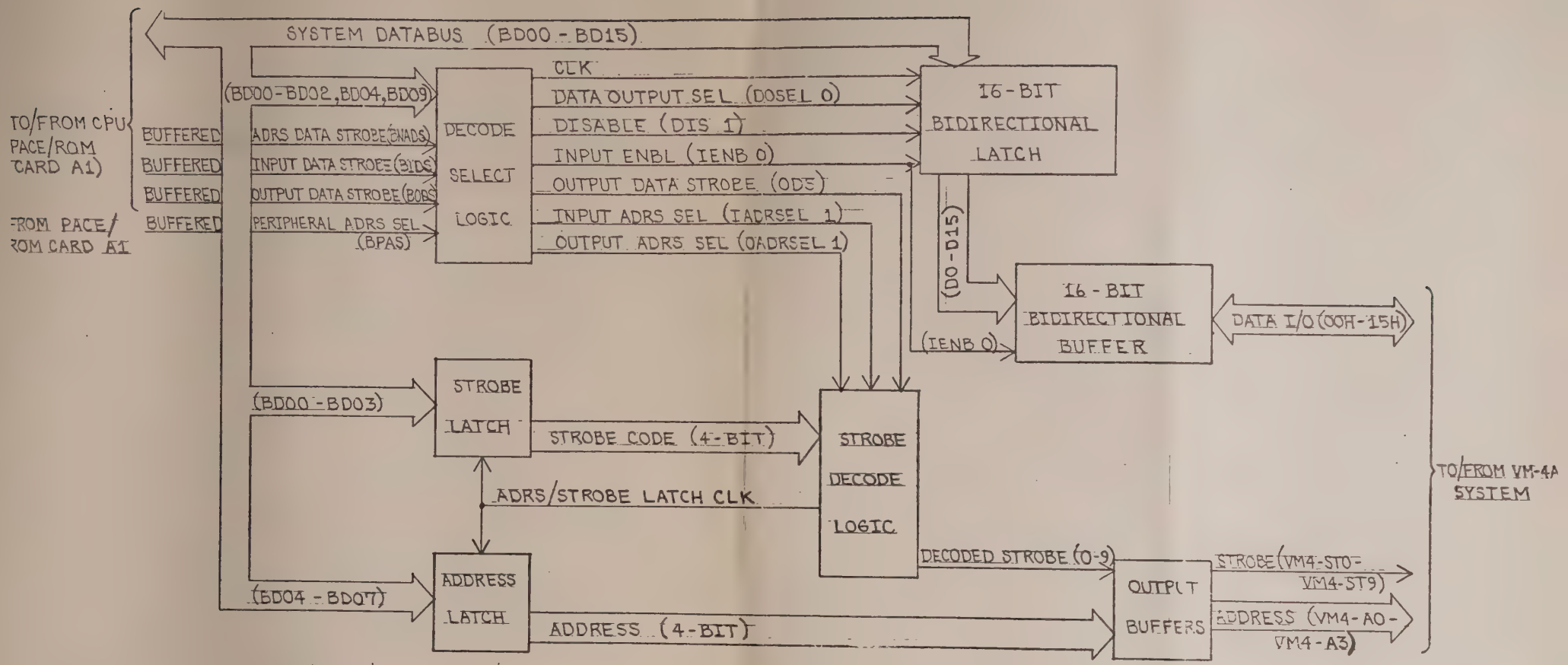


Figure 4-5, Command/Data Card, A9A5, Block Diagram

4.7.2 Data Transfer I/O Control (Continued)

Data from the CPU is sent over the system databus lines (BD00-BD15) and entered into the 16-bit bidirectional latch when signal DOSEL0 goes low. When signals DOSEL0 and DIS1 both go high, the CPU data is output to the 16-bit bidirectional buffer and sent to the VM-4A system over data lines 00H thru 15H.

Data from the VM-4A system is sent over data lines 00H thru 15H to the 16-bit bidirectional buffer, and entered into the 16-bit bidirectional latch when signal IENB0 goes low. When IENB0 goes high, the data is output to the CPU.

4.7.3 Address/Strobe Data Control

Timing for address/strobe data control is provided by the 6.25 us clock from the PACE/ROM card. The address/strobe latch clock is derived from this input.

The CPU generated VM-4A system device address (BD04-BD07) and strobe code (BD00-BD03) are applied to the address latch and strobe latch, respectively. The device address is applied through an output buffer to the VM-4A system over address lines VM4-A0 thru VM4-A3.

Only one strobe is active during a specified data transfer. The required strobe is decoded and applied through an output buffer to the VM-4A system over the applicable strobe line (VM4-ST0 - VM4-ST9). During data transfers

4.7.3 Address/Strobe Data Control (Continued)

to the CPU, the output data strobe (ODS) and input address select (IADRSEL1) signals are high. During data transfers to the VM-4A system the ODS and output address select (OADRSEL1) signals are high.

4.8 L.E.D. PARALLEL I/O CARD A7 (Figures 4-6 and 5-11)

The L.E.D. parallel I/O card converts information on the system databus into drive signals which light LEDs on the VM-4A system front panel to indicate operating status and operator interaction. The card contains buffers, an address decoder, bank select decode logic, two output banks, and an input bank.

4.8.1 Address Decoder

The address bits (BD04-BD15) on the system databus are buffered and strobed into the address decoder. They are compared to the preselected address field, and if the compare bit values coincide, the decoder compare output latches high, enabling the bank select decode logic.

4.8.2 Bank Select Decode Logic

A 3-bit bank address code (BD00-BD03) from the system databus is strobed into the bank select decode logic. This is decoded and the applicable bank is selected. If output bank 1 or 2 is selected, the buffered output data strobe (BODS) signal goes high and the LED drive signals are sent to the

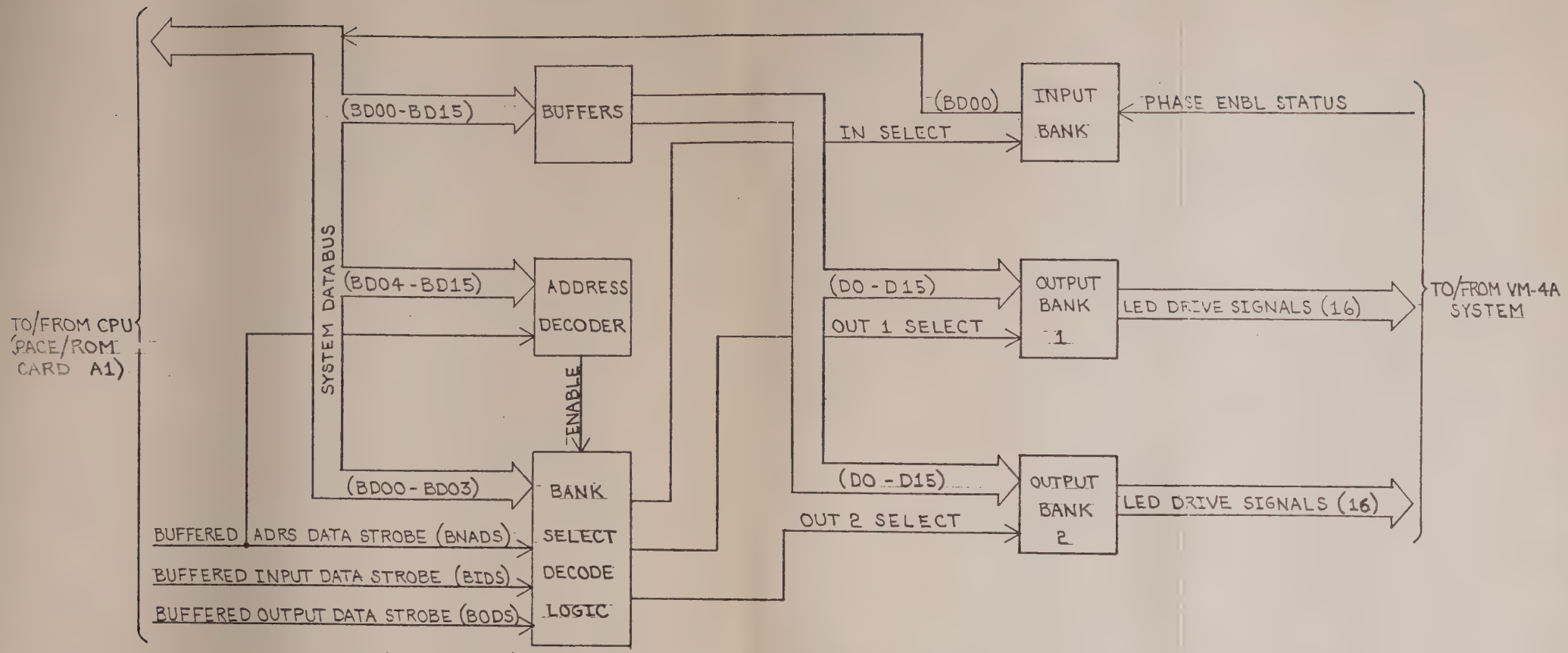


Figure 4-6,
L.E.D. Parallel I/O Card,
A9A7, Block Diagram

4.8.2 Bank Select Decode Logic (Continued)

VM-4A system. If the input bank is selected, the buffered input data strobe (BIDS) signal goes high and information from the VM-4A system is sent to the CPU over the databus. The information in this case is a phase enable status signal that informs the CPU if the phase measurement device in the VM-4A system is installed or not.

4.9 IEEE INTERFACE CARD A8 (Figures 4-7 and 5-13)

The IEEE interface card provides the interface between the CPU and an input/output (I/O) bus which conforms to the standard for IEEE communication.

The card contains address storage and decode logic, a control register, I/O bus transceivers, a talk data buffer, a talk sequencer, a listen sequencer, a listen data buffer, NIR20 interrupt logic, and a status word buffer.

4.9.1 Address Storage and Decode Logic

The card is addressed by the CPU when the buffered peripheral address select (BPAS) signal and databus line BD08 go high. When this occurs, the bits on databus lines BD00 and BD01 are strobed into the logic by the buffered address data strobe (BNADS) from the CPU. The status of bits BD00 and BD01 are decoded and the buffered input data strobe (BIDS) and buffered output data strobe (BODS) pulses from the CPU are gated out on the appropriate control lines (NIERDB, NIESES, NIETSS, NIELXB, NIECRS).

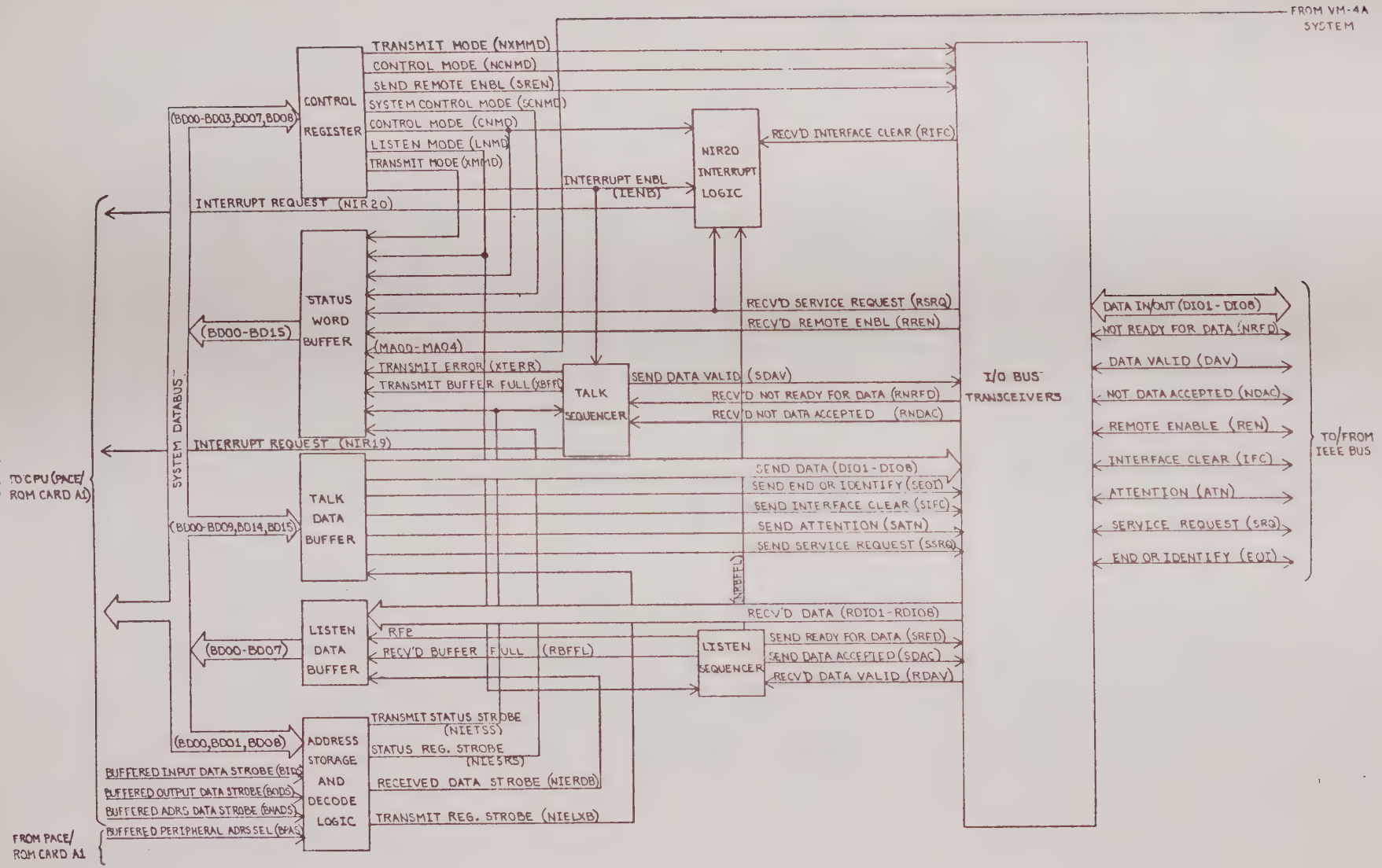


Figure 4-7,
IEEE Interface Card,
A9A8, Block Diagram

4.9.2 Control Register

The CPU transfers information via the databus (BD00-BD03, BD07, BD08) to the control register to define the control and transfer modes of the card. The card can function as the IEEE bus controller and/or the system controller. It can also be the talker or listener or both of these transfer modes can be reset. The control register also provides storage for the bit which controls the remote enable (REN) line of the IEEE bus when the card functions as the system controller.

4.9.3 I/O Bus Transceivers

The I/O bus transceivers (receiver/drivers) provide a bidirectional interface between the card and the IEEE bus. Three types of signals are applied to the interface: data (DI01-DI08), data transfer (NDAC, NRFD, DAV), and control (SRQ, ATN, IFC, REN). Control signal transmit mode (NXMMD) goes low when the card is in the talk mode and enables the transceiver drivers. Control signal control mode (NCNMD) goes low when the card is the IEEE bus controller and enables the transceiver drivers. The transceivers are continuously enabled for the listen and data transfer modes.

4.9.4 Talk Data Buffer

The CPU transfers data characters and data management bits to the talk data buffer. When the card is in the talk mode, transfer of a data character to the talk data buffer causes a character transmission sequence to be initiated. Data management bits transferred to the talk data buffer control the IEEE bus end or identify (EOI) line if the interface is in the talk mode, and the attention (ATN), service request (SRQ), and interface clear (IFC) lines if the card is functioning as bus controller.

4.9.5 Talk Sequencer

During a character transmission on the IEEE bus, the talk sequencer controls the data valid (DAV) signal and accepts the not ready for data (NRFD) and not data accepted (NDAC) signals. When the transmitted character has been accepted, the talk sequencer initiates an NIR19 interrupt request to the CPU. The routine that services this request reads the status word from the status word buffer and evaluates the transmit error (XTERR) bit from the talk sequencer to verify that the transmission has been successfully completed.

4.9.6 Listen Data Buffer

The listen data buffer stores information received from the IEEE bus via the I/O bus transceivers. The data on lines RDI01 thru RDI08 is clocked into the listen data buffer when signal RF2 from the listen sequencer goes high. The data is gated out to the CPU on databus lines BD00 thru BD07 when the received data strobe signal (NIERDB) from the address storage and decode logic goes low.

4.9.7 Listen Sequencer

When the interface is in the listen mode, the listen sequencer controls data transfer by controlling the NRFD and NDAC signals to the IEEE bus, and accepting the DAV signal from the bus. It loads the received character into the listen data buffer (RF2 high) and causes the NIR20 interrupt logic

4.9.7 Listen Sequencer (Continued)

to initiate the NIR20 interrupt request to the CPU when the received buffer full signal (NRBFFL) goes low. The routine that services this interrupt request reads the character from the listen data buffer and resets the interrupt request.

4.9.8 NIR20 Interrupt Logic

An NIR20 interrupt request is supplied to the CPU when signal NRBFFL goes low, indicating information received on the IEEE bus has been loaded into the listen data buffer, and also if an SRQ or IFC signal is received on the bus. The servicing routine reads the status word from the status word buffer to determine the cause of the interrupt.

4.9.9 Status Word Buffer

The status word is gated onto databus lines BD00 thru BD15 in response to the status register strobe (NIESRS) or transmit status strobe (NIETSS) signal going low. The status word consists of the following information bits: listen mode (LNMD), transmit mode (XMMD), control mode (CNMD), system control mode (SCNMD), received buffer full (RBFFL), transmit buffer full (XBFFL), transmit error (XTERR), received remote enable (RREN), interrupt enable (IENB), received service request (RSRQ), interface clear (EIFC), and the assigned card address (MA00-MA04).

4.9.10 Pin List - Motherboard Connections

PIN LIST

Mother Board Connections

A1 J1

PIN	SIGNAL	NOTES
1	NIR23	Extended Interrupt
2	BPAS	I/O Port Address is Selected
3	NIR17	
4	NIR16	
5	NIR22	
6	NIR19	
7	NIR18	
8	NIR21	
9	TTLCLK	
10	NIR20	
11	BNVAD	
12	BPCYC	3.125 μsec Clock
13	DCPOK	H02 on
14	INIT	
15	NINIT	
16	BNHALT	Only to A2 J2 - 24
17	BLZAC	Only to A2 J2 - 20
18		Not Used
19	BPH4	JC 13 also to A2 J2 - 45 used only to clock extended interrupts
20	BF14	
21	BF11	
22	BF13	
23	BF12	
24	BDIS	
25	BD15	
26		No Connection

PIN LIST

Mother Board Connections

A1 J1

PIN	SIGNAL	NOTES
27	BD14	
28		No Connection
29	BD13	
30		No Connection
31	BD12	
32		No Connection
33	BD11	
34		No Connection
35	BD10	
36		No Connection
37	BDØ9	
38		No Connection
39	BDØ8	
40		No Connection
41	BDØ7	
42		No Connection
43	BDØ6	
44		No Connection
45	BDØ5	
46	EXTEND	Grounded
47	BDØ4	
48	BPS	To P5V only
49	BDØ3	
50	BNLZRQ	To A2 J2 - 32 only (not used)
51	BDØ2	
52	B CONTIN	to A2 J2 - 28 Only (not used)
53	BDØ1	

PIN LIST

Mother Board Connections

A1 J1

PIN	SIGNAL	NOTES
54	NIR3	
55	BDØØ	
56	BIDS	
57	BNADS	
58	BODS	
59	NIR4	
60	NIR2	
61	JC13	
62	JC15	
63	GND	
64	GND	
65	-12V	
66	-12V	
67	+5V	
68	+5V	
69	GND	
70	GND	

PIN LIST

Mother Board Connections

A1 J2

PIN	SIGNAL	NOTES
1		No Connection
2		
3		
4		
5		
6		
7		
8		
9		
10		
11		
12		
13		
14		
15		
16		
17		
18		
19		
20		
21		
22		
23		
24		
25		
26		No Connection

PIN LIST

Mother Board Connections

A1 J2

PIN	SIGNAL	NOTES
27		No Connection
28		
29		
30		
31		
32		
33		
34		
35		
36		
37		
38		
39		
40		
41		
42		
43		
44		
45		
46		No Connection
47	NAMDOE	5.12 MHz tied to Pin 53
48		No Connection
49	5.12 MHz	Unbuffered tied to pin 51
50		No Connection
51	5.12 MHz	
52		No Connection
53	5.12 MHz	Buffered

PIN LIST

Mother Board Connections

A1 J2

PIN	SIGNAL	NOTES
54		No Connection
55	2.56 MHz	
56		No Connection
57	1.56 μsec	.64 MHz
58		No Connection
59	6.25 μsec	To Command/Data Card P2 - 10
60		No Connection
61	12.5 μsec	
62		No Connection
63		
64		
65		
66		No Connection
67	P5V	
68	P5V	
69	GND	
70	GND	

PIN LIST

Mother Board Connections

A2 - A7 J1

PIN	SIGNAL	NOTES
1	NIR23	RS-232 Interrupt
2	BPAS	Peripheral Address Select
3	NIR17	
4	NIR16	
5	NIR22	
6	NIR19	IEEE XMIT Comp. Interrupt
7	NIR18	
8	NIR21	
9	TTLCLK	1.28 MHz (not used)
10	NIR20	IEEE General Interrupt
11	BNVAD	Address Recognized Response (not used in VM-4A)
12	BPCYC	3.125 μsec Clock used in IEEE Interface
13	DCPOK	External Initialize - used for H02 on Signal
14	INIT	
15	NINIT	
16		Not Used
17		Not Used
18		Not Used
19	BPH4	JC13 used only on A1
20	BF14	
21	BF11	
22	BF13	
23	BF12	
24	BDIS	Bus Disable (not used)
25	BD15	
26		Not Used

PIN LIST

Mother Board Connections

A2 - A7 J1

PIN	SIGNAL	NOTES
27	BD14	
28	GND	
29	BD13	
30	GND	
31	BD12	
32	GND	
33	BD11	
34	GND	
35	BD1Ø	
36	GND	
37	BDØ9	
38	GND	
39	BDØ8	
40	GND	
41	BDØ7	
42	GND	
43	BDØ6	
44	GND	
45	BDØ5	
46	GND	
47	BDØ4	
48	GND	
49	BDØ3	
50	GND	
51	BDØ2	
52	GND	
53	BDØ1	

PIN LIST

Mother Board Connections

A2 - A7 J1

PIN	SIGNAL	NOTES
54	NIR3	Real time interrupt
55	BDØØ	
56	BIDS	Input Data Strobe
57	BNADS	Address Strobe
58	BODS	Output Data Strobe
59	NIR4	Keyboard Data Interrupt
60	NIR2	L.O. Interrupt
61	JC13	Not Used
62	JC15	Not Used
63	+12V	
64	+12V	
65	-12V	
66	-12V	
67	+5V	
68	+5V	
69	GND	
70	GND	

PIN LIST

Mother Board Connections

A2 J2

PIN	SIGNAL	NOTES
		All pins on this socket are used for the external Bus Buffer option not utilized in this system.

PIN LIST

Mother Board Connections

A3 J2

PIN	SIGNAL	NOTES
1	Display Data Ø4	
2		Not Used
3	Display Data Ø3	
4	Display Data Ø5	
5	Display Data Ø1	
6	Display Data Ø6	
7	Display Data Ø2	
8		No Connection
9		No Connection
10	Display CLK	
11		No Connection
12	Scan Disable	
13		No Connection
14	Display Update Clock	From Display
15		No Connection
16	Display Reset	
17		No Connection
18		
19		
20		
21		
22		
23		
24		
25		
26		No Connection

PIN LIST

Mother Board Connections

A3 J2

PIN	SIGNAL	NOTES
27	SHF	Shift Key (not used)
28	Repeat Out	10 Hz Clock (not used)
29	Y7	
30	Y1Ø	
31	Y5	
32	Y8	
33	Y6	
34	Y9	
35	X7	
36	SHF LOCK	Shift Lock Key (not used)
37	X6	
38	Cont	Control Key (not used)
39		Not Used
40		Not Used
41	Repeat In	
42		Not Used
43	X2	
44	X1	
45	Y3	
46	Y4	
47		Not Used
58	X5	
49	Y2	
50	Y1	
51	X4	
52	X3	
53	X8	

PIN LIST

Mother Board Connections

A3 J2

PIN	SIGNAL	NOTES
54	X9	
55	Sonalert Drive	
56		Not Used
57		
58		
59		
60		
61		
62		
63		
64		Not Used
65	-12V	
66	-12V	
67	+5V	
68	+5V	
69	GND	
70	GND	

PIN LIST

Mother Board Connections

A4 J2

PIN	SIGNAL	NOTES
1		Not Used
2	GND	
3		Not Used
4	RS-232 Out	Serial Data Out
5		Not Used
6	RS-232 In	Serial Data In
7		Not Used
8	RTS	Request to Send
9		Not Used
10	CTS	Clear to Send
11		Not Used
12	DSR	Data Set Ready
13	Jumper To GND	
14		Not Used
15	RLSD	Received Line Detect
16	DTR	Data Term Ready
17	OUT1	Aux. Output EIA
18		Not Used
19	RI	Ring Indicator
20		Not Used
21		
22		
23		
24		
25		
26		Not Used

PIN LIST

Mother Board Connections

A4 J2

PIN	SIGNAL	NOTES
27		Not Used
28		
29		
30		
31		Not Used
32	GND	
33		Not Used
34	See 6	
35		Not Used
36	See 4	
37		Not Used
38	See 10	
39	TTY Keyboard	P12V
40	See 8	
41	TTY Keyboard	N12V
42	See 16	
43	Jumper	See 13
44		Not Used
45	See 17	
46	See 12	
47	See 15	
48		Not Used
49	+ TTY Printer	20 Ma Loop
50	OUT2	Aux. output TTL
51	-TTY Printer	20 Ma Loop
52		Not Used
53	+P.T.RDR	20Ma Loop

PIN LIST

Mother Board Connections

A4 J2

PIN	SIGNAL	NOTES
54		Not Used
55	-P.T.RDR	20 Ma Loop
56		Not Used
57		Not Used
58		Not Used
59	2.56 MHz	From A1 J2 - 55
60		Not Used
61		Not Used
62		Not Used
63	+12V	
64	+12V	
65	-12V	
66	-12V	
67	+5V	
68	+5V	
69	GND	
70	GND	

PIN LIST

Mother Board Connections

A5 J2

PIN	SIGNAL	NOTES
1		Not Used
2		
3		
4		
5		
6		
7		
8		
9		Not Used
10	6.25 μs CLK	From A1 J2 - 59
11		Not Used
12	IENBØ	
13		Not Used
14		
15		
16		
17		
18		
19		
20		
21		
22		
23		Not Used
24	BIR3	To NIR2 at A5 J1 - 60
25		Not Used
26		Not Used

PIN LIST

Mother Board Connections

A5 J2

PIN	SIGNAL	NOTES
27	DCPOK	H02 on to A5 J1 - 13
28	LO INT	
29		Not Used
30		Not Used
31	VM4AØ	VM4 Address Ø
32	VM4A1	VM4 Address 1
33	VM4A2	VM4 Address 2
34	VM4A3	VM4 Address 3
35	VM4STØ	VM4 Strobe Ø
36	VM4ST1	VM4 Strobe 1
37	VM4ST2	VM4 Strobe 2
38	VM4ST3	VM4 Strobe 3
39	VM4ST4	VM4 Strobe 4
40	VM4ST5	VM4 Strobe 5
41	VM4ST6	VM4 Strobe 6
42	VM4ST7	VM4 Strobe 7
43	VM4ST8	VM4 Strobe 8
44	VM4ST9	VM4 Strobe 9
45	VM4ST10	VM4 Strobe 10
46	VM4ST11	VM4 Strobe 11
47	VM4ST12	VM4 Strobe 12
48	VM4ST13	VM4 Strobe 13
49	VM4ST14	VM4 Strobe 14
50	VM4ST15	VM4 Strobe 15
51	DIO ØØ	VM4 I/O Data
52	DIO Ø1	VM4 I/O Data
53	DIO Ø2	VM4 I/O Data

PIN LIST

Mother Board Connections

A5 J2

PIN	SIGNAL	NOTES
54	DIO Ø3	VM4 I/O Data
55	DIO Ø4	
56	DIO Ø5	
57	DIO Ø6	
58	DIO Ø7	
59	DIO Ø8	
60	DIO Ø9	
61	DIO 1Ø	
62	DIO 11	
63	DIO 12	
64	DIO 13	
65	DIO 14	
66	DIO 15	VM4 I/O Data
67	+5V	
68	+5V	
69	GND	
70	GND	

PIN LIST

Mother Board Connections

A7 J2

PIN	SIGNAL	NOTES
1		Not Used
2	DATA IN Ø	Input Ø (Phase inst.)
3		Not Used
4	DATA IN 1	Input 1
5		Not Used
6	DATA IN 2	Input 2
7		Not Used
8	DATA IN 3	Input 3
9		Not Used
10	DATA IN 4	Input 4
11		Not Used
12	DATA IN 5	Input 5
13		Not Used
14	DATA IN 6	Input 6
15		Not Used
16	DATA IN 7	Input 7
17		Not Used
18	DATA IN 8	Input 8
19		Not Used
20	DATA IN 9	Input 9
21		Not Used
22	DATA IN 10	Input 10
23		Not Used
24	DATA IN 11	Input 11
25		Not Used
26	DATA IN 12	Input 12

PIN LIST

Mother Board Connections

A7 J2

PIN	SIGNAL	NOTES
27		Not Used
28	DATA IN 13	Input 13
29		Not Used
30	DATA IN 14	Input 14
31		Not Used
32	DATA IN 15	Input 15
33	BANK 1 OUT Ø	LED
34	BANK 2 OUT Ø	LED
35	BANK 1 OUT 1	
36	BANK 2 OUT 1	
37	BANK 1 OUT 2	
38	BANK 2 OUT 2	
39	BANK 1 OUT 3	
40	BANK 2 OUT 3	
41	BANK 1 OUT 4	
42	BANK 2 OUT 4	
43	BANK 1 OUT 5	
44	BANK 2 OUT 5	
45	BANK 1 OUT 6	
46	BANK 2 OUT 6	
47	BANK 1 OUT 7	
48	BANK 2 OUT 7	
49	BANK 1 OUT 8	
50	BANK 2 OUT 8	
51	BANK 1 OUT 9	
52	BANK 2 OUT 9	
53	BANK 1 OUT 10	
54	BANK 2 OUT 10	LED

PIN LIST

Mother Board Connections

A7 J2

PIN	SIGNAL	NOTES
55	BANK 1 OUT 11	LED
56	BANK 2 OUT 11	
57	BANK 1 OUT 12	
58	BANK 2 OUT 12	
59	BANK 1 OUT 13	
60	BANK 2 OUT 13	
61	BANK 1 OUT 14	
62	BANK 2 OUT 14	
63	BANK 1 OUT 15	
64	BANK 2 OUT 15	LED
65	DATA IN CLOCK	Tied to EIDS
66	CLEAR OUTPUT	Not Used
67	+5V	
68	+5V	
69	GND	
70	GND	

PIN LIST

Mother Board Connections

A8 J2

PIN	SIGNAL	NOTES
1	SRQ	
2	ATN	
3	NDAC	
4	IFC	
5	DAV	
6	NRFD	
7	DIO 4	IEEE DATA BUS
8	EOI	
9	DIO 2	IEEE DATA BUS
10	DIO 3	
11	DIO 5	
12	DIO 1	
13	DIO 7	
14	DIO 6	IEEE DATA BUS
15	REN	
16	DIO 8	IEEE DATA BUS
17	GNRFD	
18	GNDAV	
19	GIFC	
20	GNDAC	
21	MAØØ	IEEE DEVICE ADDRESS
22	MARTN	GND
23	MAØ2	IEEE DEVICE ADDRESS
24	MAØ1	
25	MAØ4	
26	MAØ3	IEEE DEVICE ADDRESS

PIN LIST

Mother Board Connections

A8 J2

PIN	SIGNAL	NOTES
27		Not Used
28		
29		
39		
31		
32		Not Used
33	RREN	
34		Not Used
35		
36		
37		
38		
39		
40		
41		
42		
43		
44		
45		
46		
47		
48		
49		
50		
51		
52		
53		Not Used

PIN LIST

Mother Board Connections

A8 J2

PIN	SIGNAL	NOTES
54		Not Used
55		
56		
57		
58		
59		
60		
61		
62		
63		
64		
65		
66		Not Used
67	+5V	
68	+5V	
69	GND	
70	GND	

PIN LIST

Mother Board Connections

A9 J3

PIN	SIGNAL	NOTES
1	GND	Power Supply Connections
2	GND	
3	GND	
4	GND	
5	GND	
6	+5V	
7	+5V	
8	+5V	
9	+5V	
10	+5V	
11	-12V	
12	Not Used	
13	Not Used	
14	Not Used	
15	Not Used	
16	Not Used	
17	Not Used	
18	Not Used	
19	+12V	
20	Not Used	

PIN LIST

Mother Board Connections

A9 J4

PIN	SIGNAL	NOTES
1	Y4	X-4 Matrix Connectors
2	Y3	for front panel pushbuttons
3	Y2	
4	Y1	
5	Y10	
6	Y5	
7	Y6	
8	Y7	
9	Y8	
10	Y9	
11	Not Used	
12	X7	
13	X6	
14	X5	
15	X4	
16	X3	
17	X2	
18	X1	

SECTION 5
SCHEMATIC DIAGRAMS
AND
ASSEMBLY DRAWINGS

This sections contains the schematic diagrams for the PACE Microprocessor, 1A9, a subsystem of the VM-4A Attenuator and Signal Generator Calibrator. The remainder of the VM-4A schematics are contained in the Operation and Service Manual for the Model VM-4A.

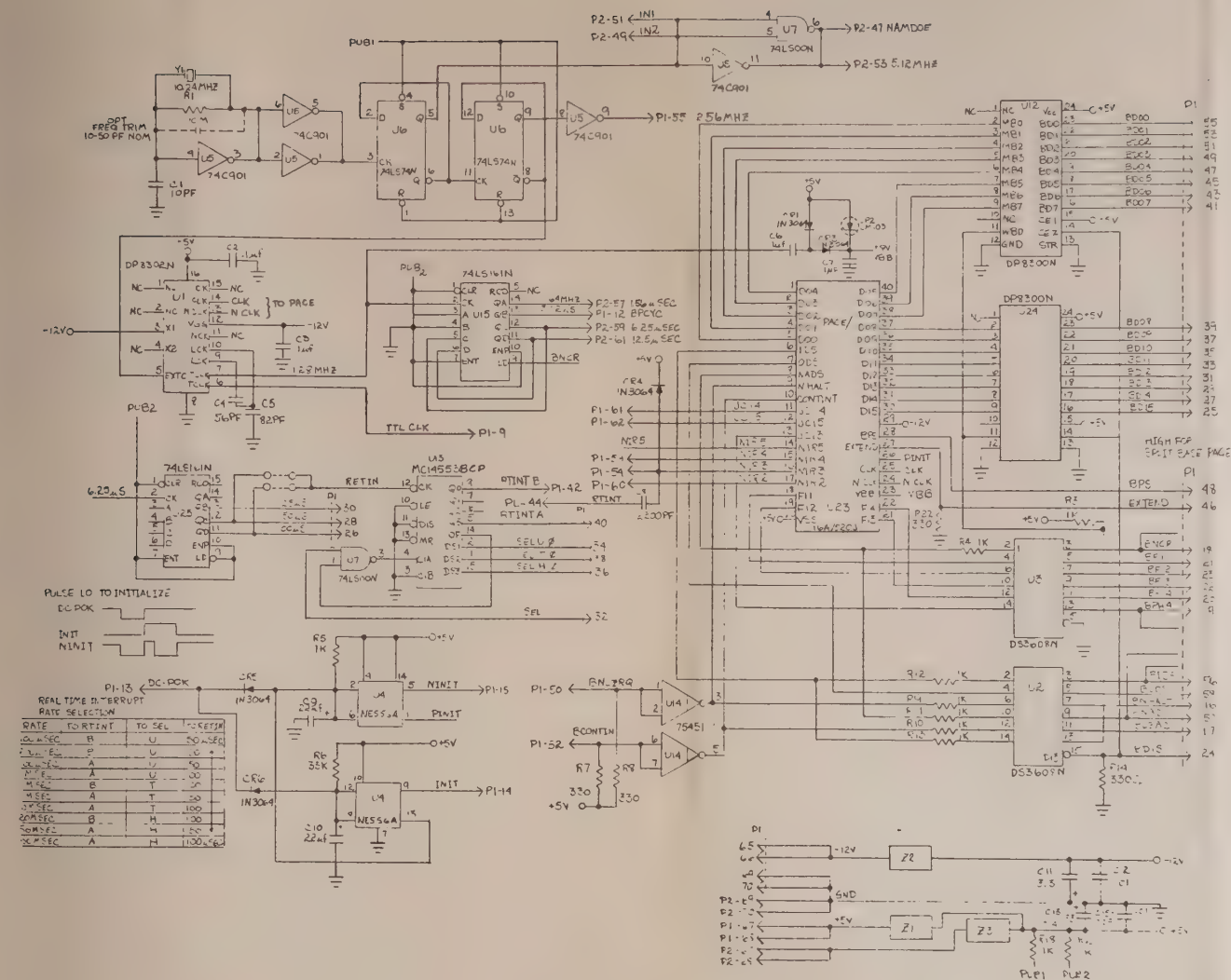
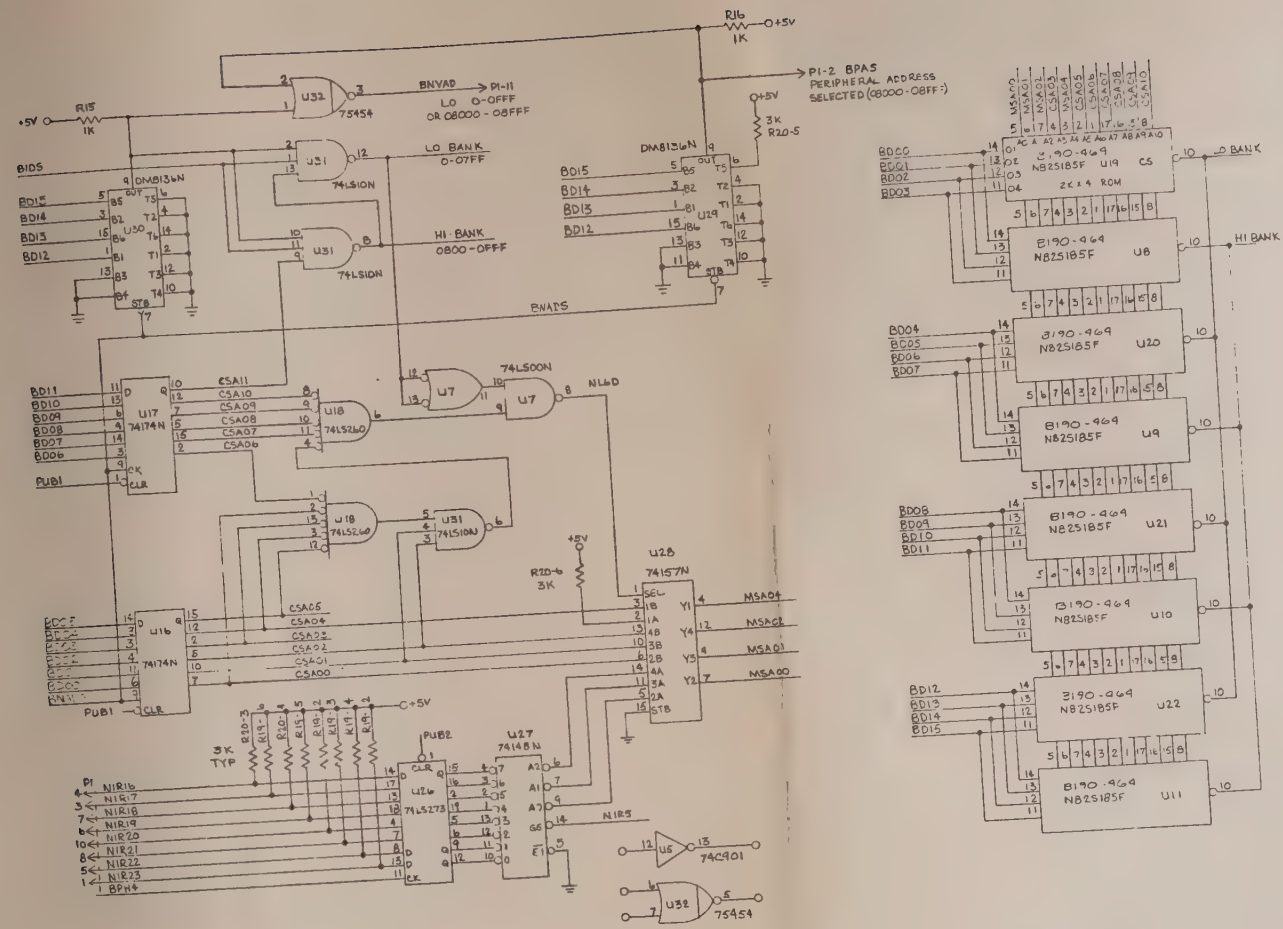
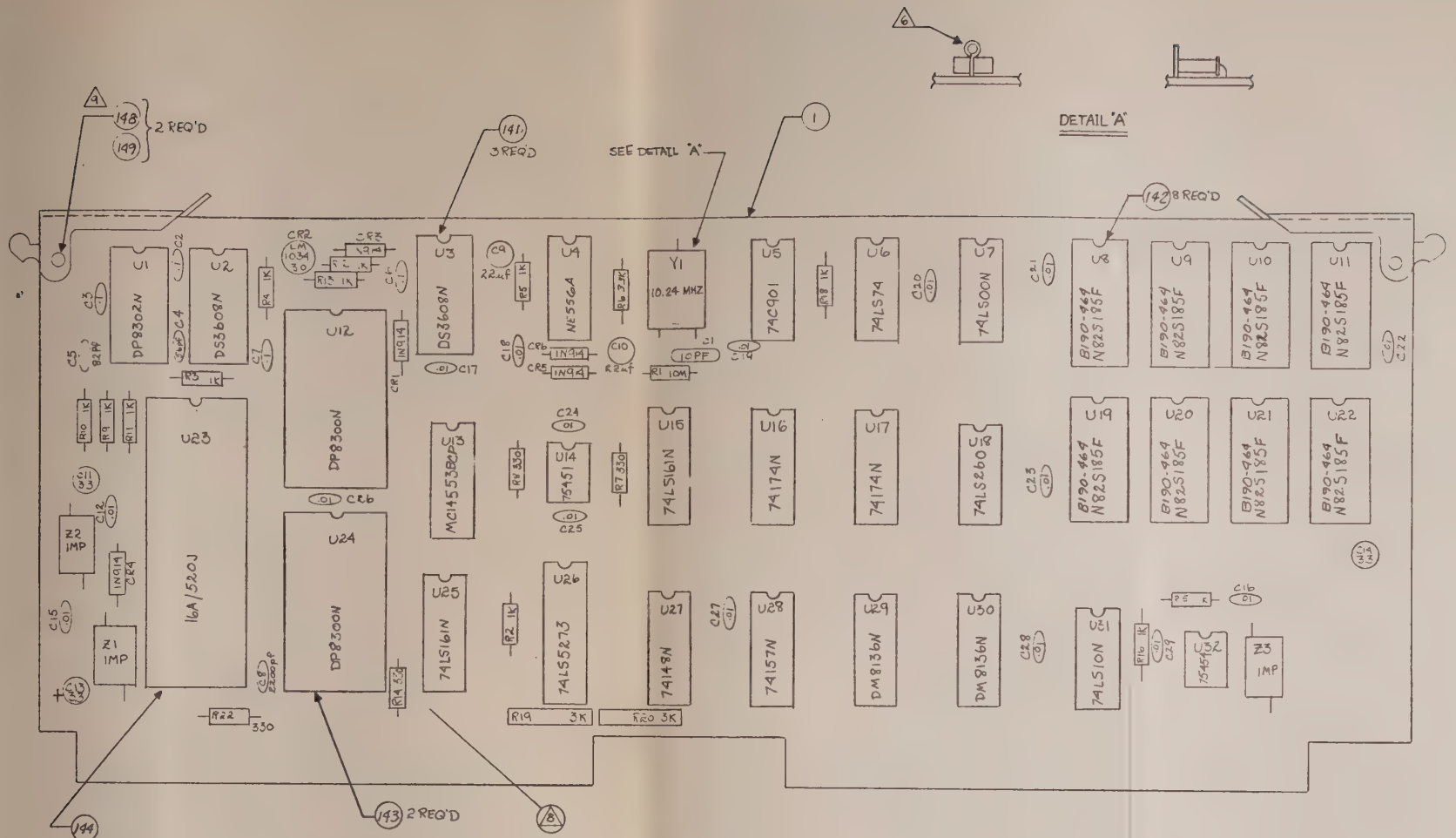


Figure 5-1
PACE/ROM Card
1A9A1, Schematic Diagram



ITS-118111-30-2-G SHT 2 OF 2

Figure 5-1
PACE/ROM Card
1A9A1, Schematic Diagram



10. (-1) SPRAY CONFORMAL COAT BOTH SIDES
9. INSTALL ITEM 66 (EJECTOR) WITH ITEM 67 (EYELET) AND SWAGE IN PLACE
8. FOR -1 VERSION JUMPER RET TO 100, -2 RET TO 50
7. DIODES ARE IN 914
6. GND TO BE SOLDERED IN LOOP TO TOP OF CRYSTAL. GND TO BE 18 GAUGE WIRE. GND MUST BE SOLDERED QUICKLY TO AVOID RUINING THE CRYSTAL
5. SEE P/90-287-2 FOR PARTS LIST
4. STAMP -1 AS PART OF ASSEMBLY PART NUMBER AS REQUIRED
3. FOR -1 VERSION DELETE U25
2. ALL CAPS IN MFD's
1. ALL RESISTORS IN OHMS ¼ 5%

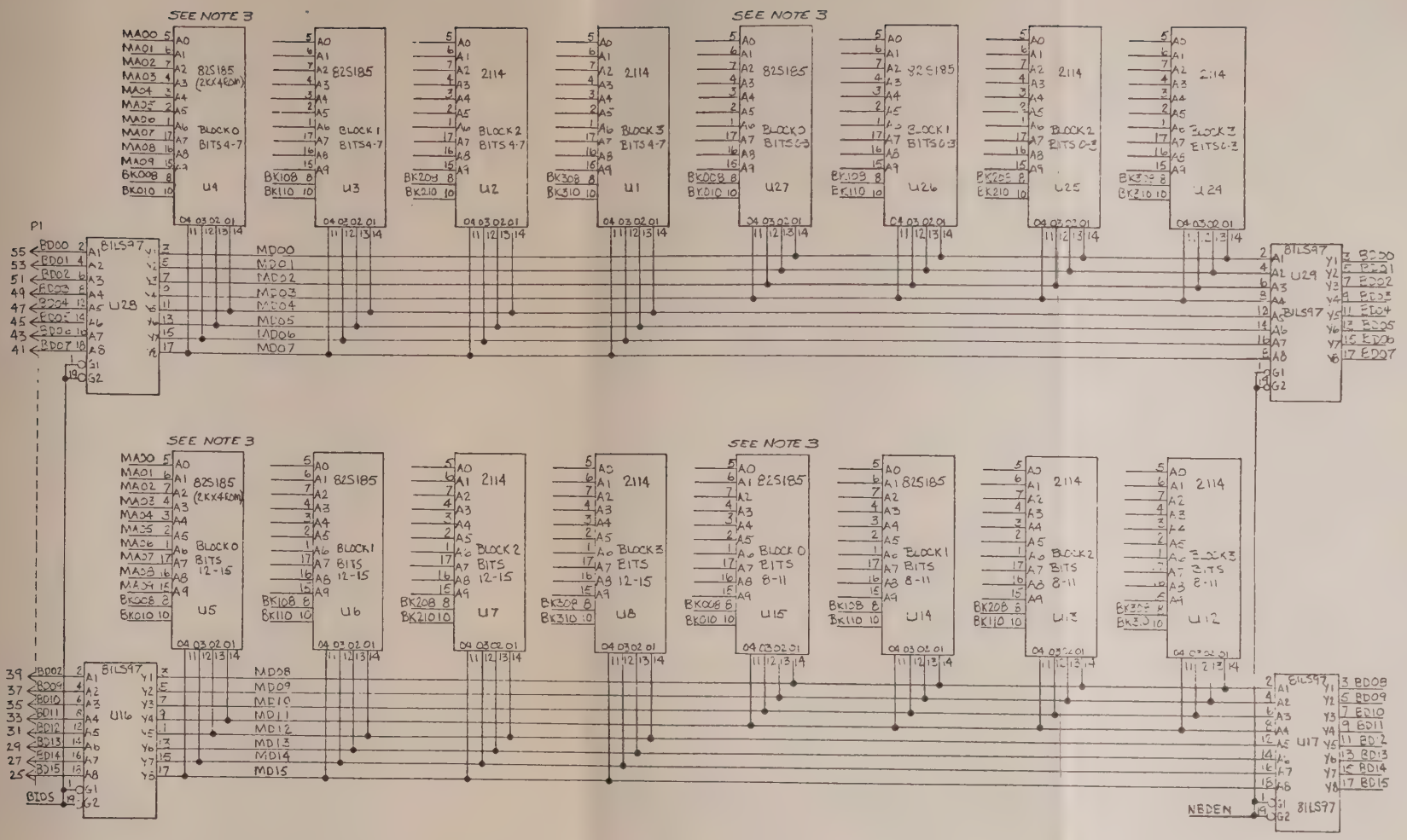
NOTES: UNLESS OTHERWISE SPECIFIED

ITS-1180111-60-M

SHT 1 OF 1

Figure 5-2
PACE/ROM Card
1A9A1, Assembly Drawing

BRUNING 40-526 32018



3 DO NOT INSTALL U4, U5, U15, U27 FOR -2 ASSY

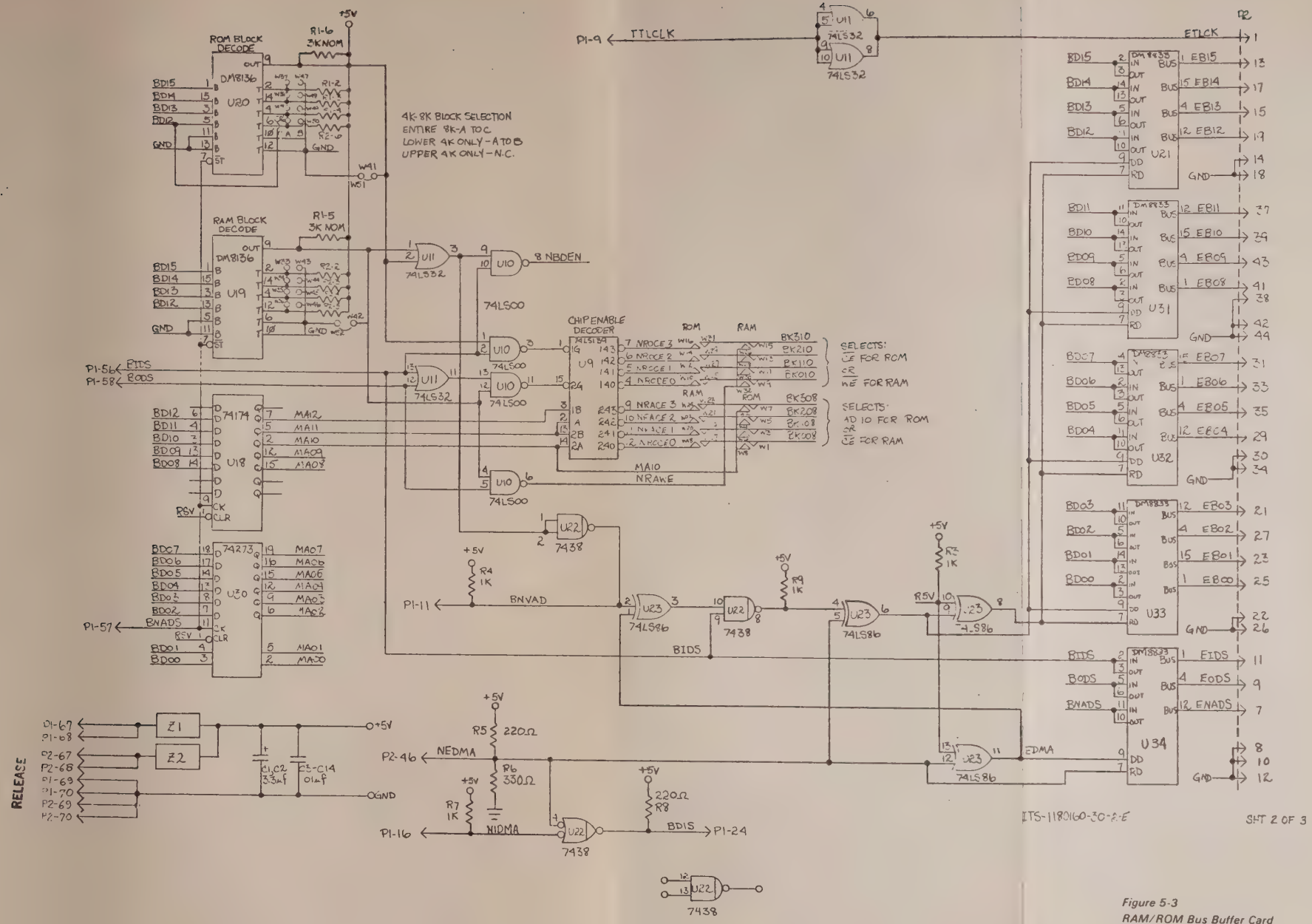
2. UNLESS OTHERWISE SPECIFIED:
   a. ALL RESISTORS IN OHMS; 1/4 W, 5%
   b. ALL CAPS IN MFD
1. SEE TABULATION (SH3) FOR APPROPRIATE JUMPERS; SEE COMPONENT LOCATION & PARTS LIST FOR APPROPRIATE VALUES/TYPES OF SELECTED COMPONENTS

NOTES:

LTS-1160160-20-1-E

SHT 1 OF 3

Figure 5-3
RAM/ROM Bus Buffer Card
1A9A2, Schematic Diagram



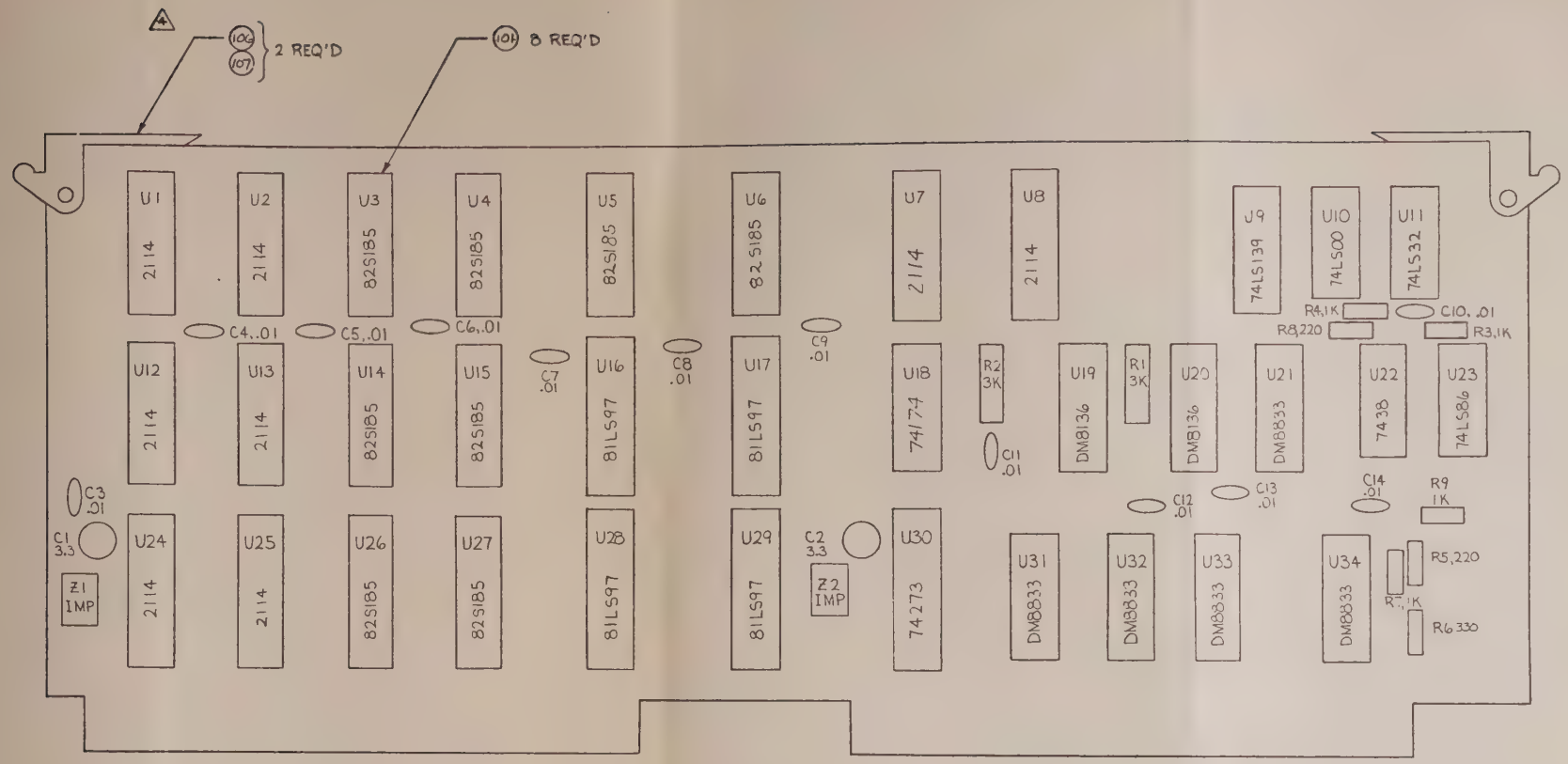
ITS-1180160-30-A.E

SHT 2 OF 3

Figure 5-3
RAM/ROM Bus Buffer Card
1A9A2, Schematic Diagram

TABULATION	
DASH NO.	JUMPERS
-1	W1 TO W2 W3 TO W4 W9 TO W14 W11 TO W16 W21 TO W22 W23 TO W24 W29 TO W30 W31 TO W32 W37 TO W47 W38 TO W48 W39 TO W49
-2	W19 TO W20 W21 TO W22 W23 TO W24 W27 TO W28 W29 TO W30 W31 TO W32 W41 TO W51

Figure 5-3
RAM/ROM Bus Buffer Card
1A9A2, Schematic Diagram



6. (-2) CONFORMAL COAT BOTH SIDES
5. INSTALL ITEM 106 (EJECTOR) WITH ITEM 107 (EYELET) AND SWAGE IN PLACE
4. THIS DRAWING IS DASH NO. 1 SEE TABULATION FOR APPROPRIATE VALUES OF SELECT COMPONENTS
3. REF. TO FL190-257-3 FOR PARTS LIST
2. ALL CAPS IN MFD'S
1. ALL RESISTORS IN OHMS, 1/4W, 5%

NOTES: UNLESS OTHERWISE SPECIFIED

ITS-1180160-00-1-F SHT 1 OF 2

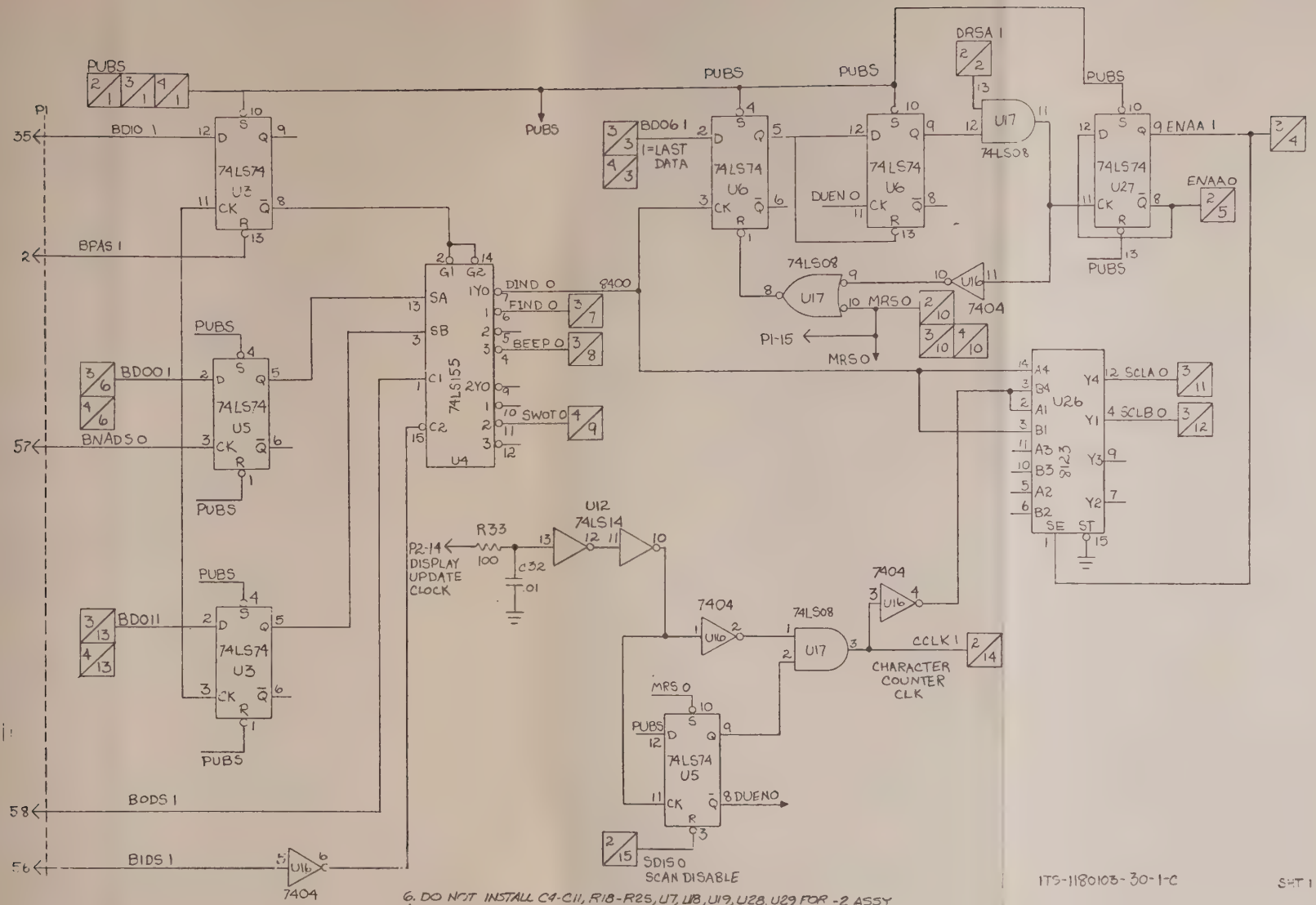
Figure 5-4
RAM/ROM Bus Buffer Card
1A9A2, Assembly Drawing

TABULATION																	
DASH NO.	COMPONENTS																
-1	U1 2114	U2 2114	U3 82S185	U4 82S185	U5 82S185	U6 82S185	U7 2114	U8 2114	U12 2114	U13 2114	U14 82S185	U15 82S185	U24 2114	U25 2114	U26 82S185	U27 82S185	
-2	U1 2114	U2 2114	U3 2114	U4 OMIT	U5 OMIT	U6 2114	U7 2114	U8 2114	U12 2114	U13 2114	U14 2114	U15 2114	U24 2114	U25 2114	U26 2114	U27 OMIT	

TABULATION	
DASH NO.	JUMPERS
-1	W1 TO W2 W3 TO W4 W9 TO W14 W11 TO W16 W21 TO W22 W23 TO W24 W29 TO W30 W31 TO W32 W37 TO W47 W38 TO W48 W39 TO W49
-2	W19 TO W20 W21 TO W22 W23 TO W24 W27 TO W28 W29 TO W30 W31 TO W32 W41 TO W51

JNING 40526 32018

Figure 5-4
RAM/ROM Bus Buffer Card
1A9A2, Assembly Drawing

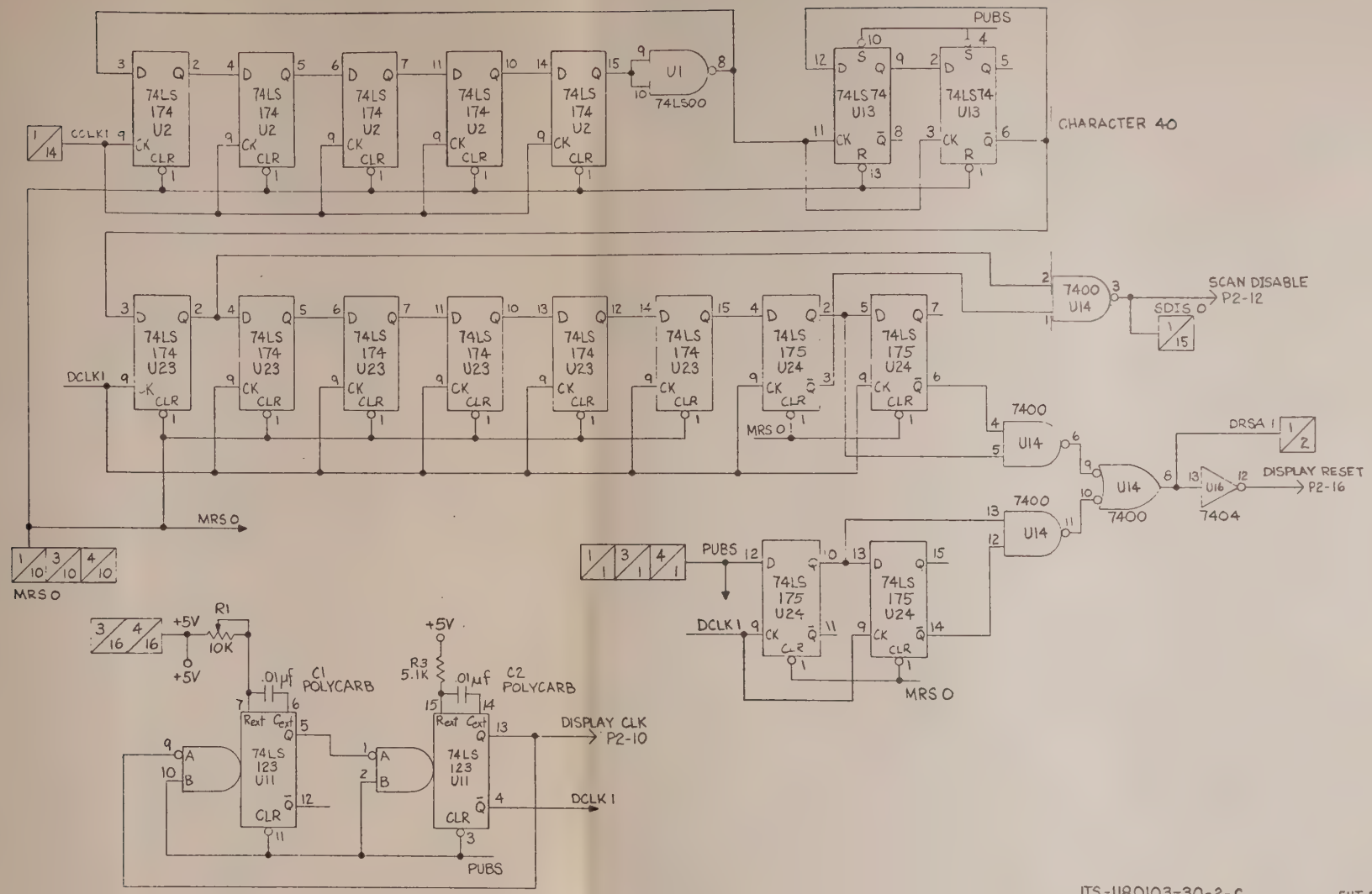


6. DO NOT INSTALL C4-C11, R18-R25, U7, U8, U19, U28, U29 FOR -2 ASSY
5. C-30 IS FOR GENERAL USE REQUIRING CURRENT LIMITING RESISTORS.
4. C-1 IS FOR 9007/9629 RANGE SIMULATOR.
3. REF. TO PL190-287-4 FOR PARTS LIST
2. ALL CAPACITORS IN UFDS
1. ALL RESISTORS 1/4 W 5%
NOTES: UNLESS OTHERWISE SPECIFIED

1TS-1180103-30-1-C

SHT 1 OF 4

Figure 5-5
Front Panel Controller Card
1A9A3, Schematic Diagram



ITS-1180103-30-2-C SHT 2 OF 4

Figure 5-5
Front Panel Controller Card
1A9A3, Schematic Diagram

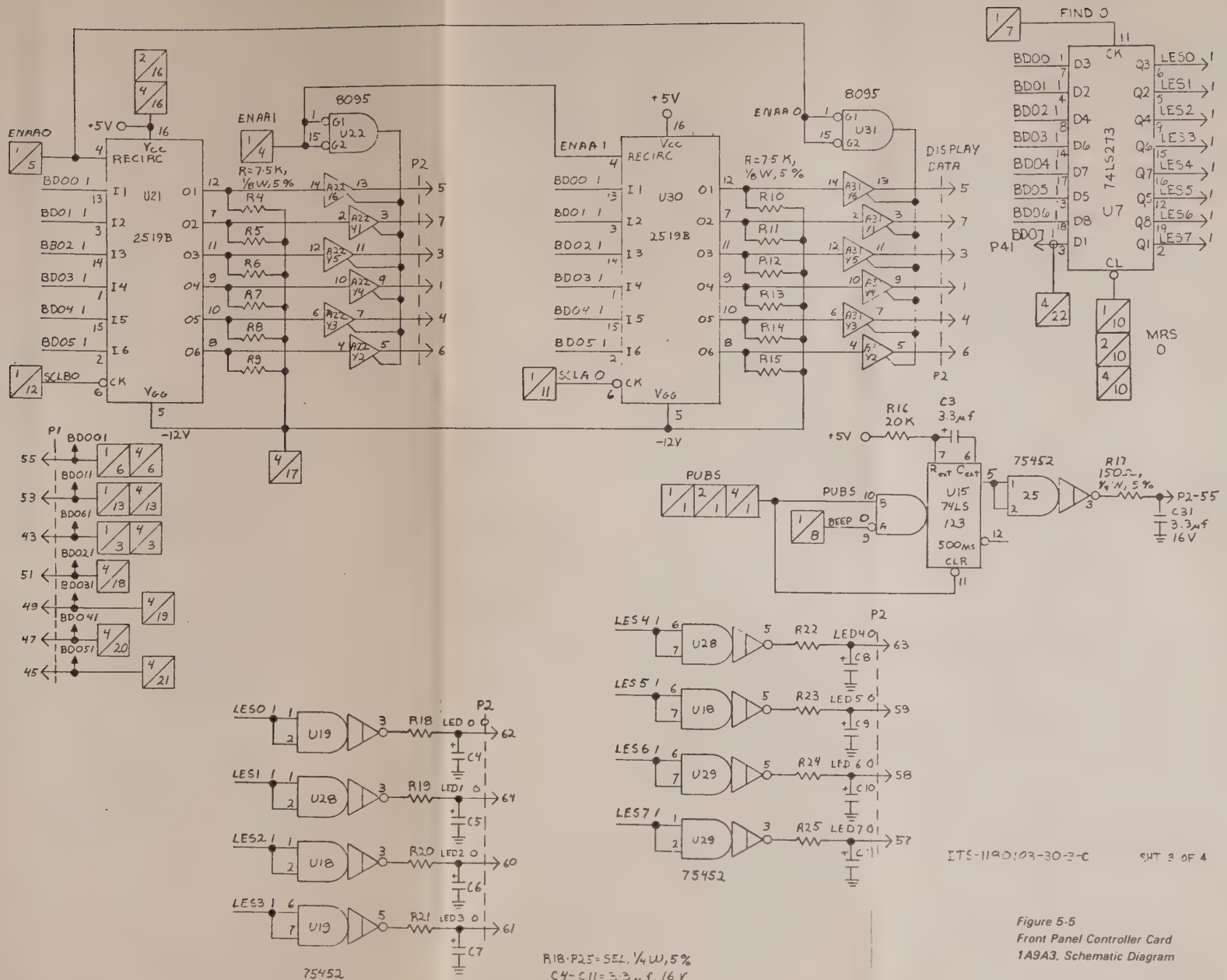


Figure 5-5
Front Panel Controller Card
1A9A3, Schematic Diagram

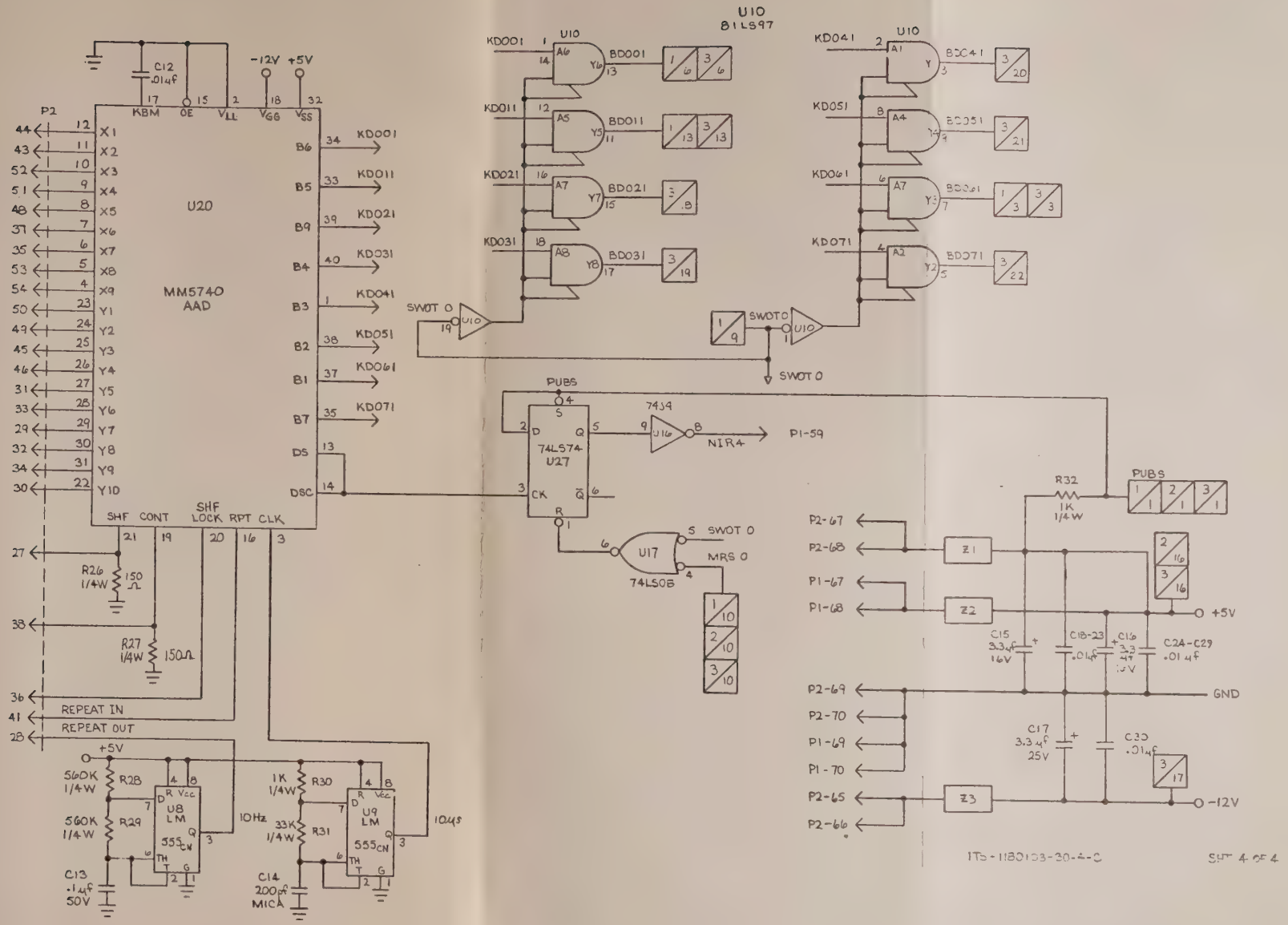
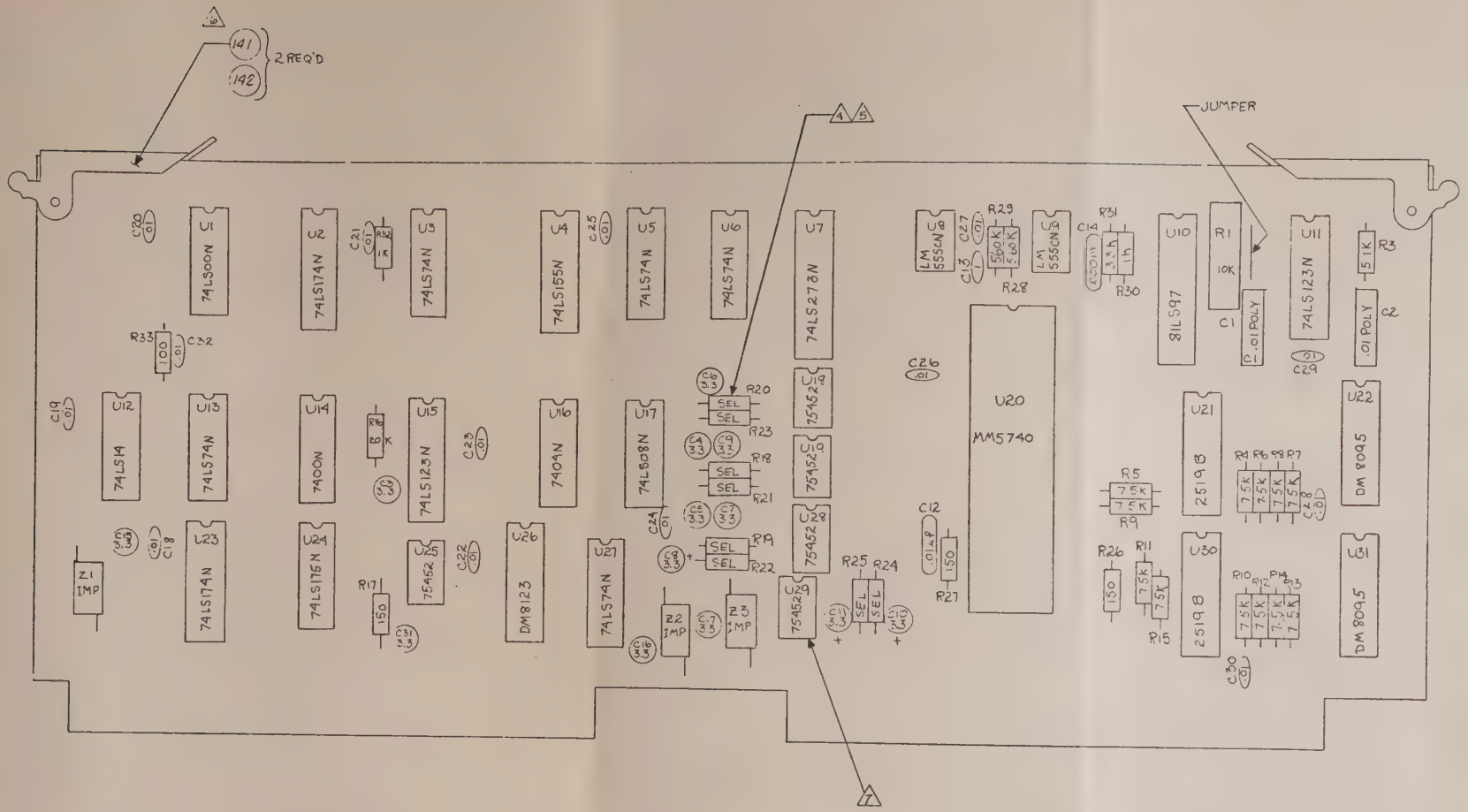


Figure 5-5
Front Panel Controller Card
1A9A3, Schematic Diagram



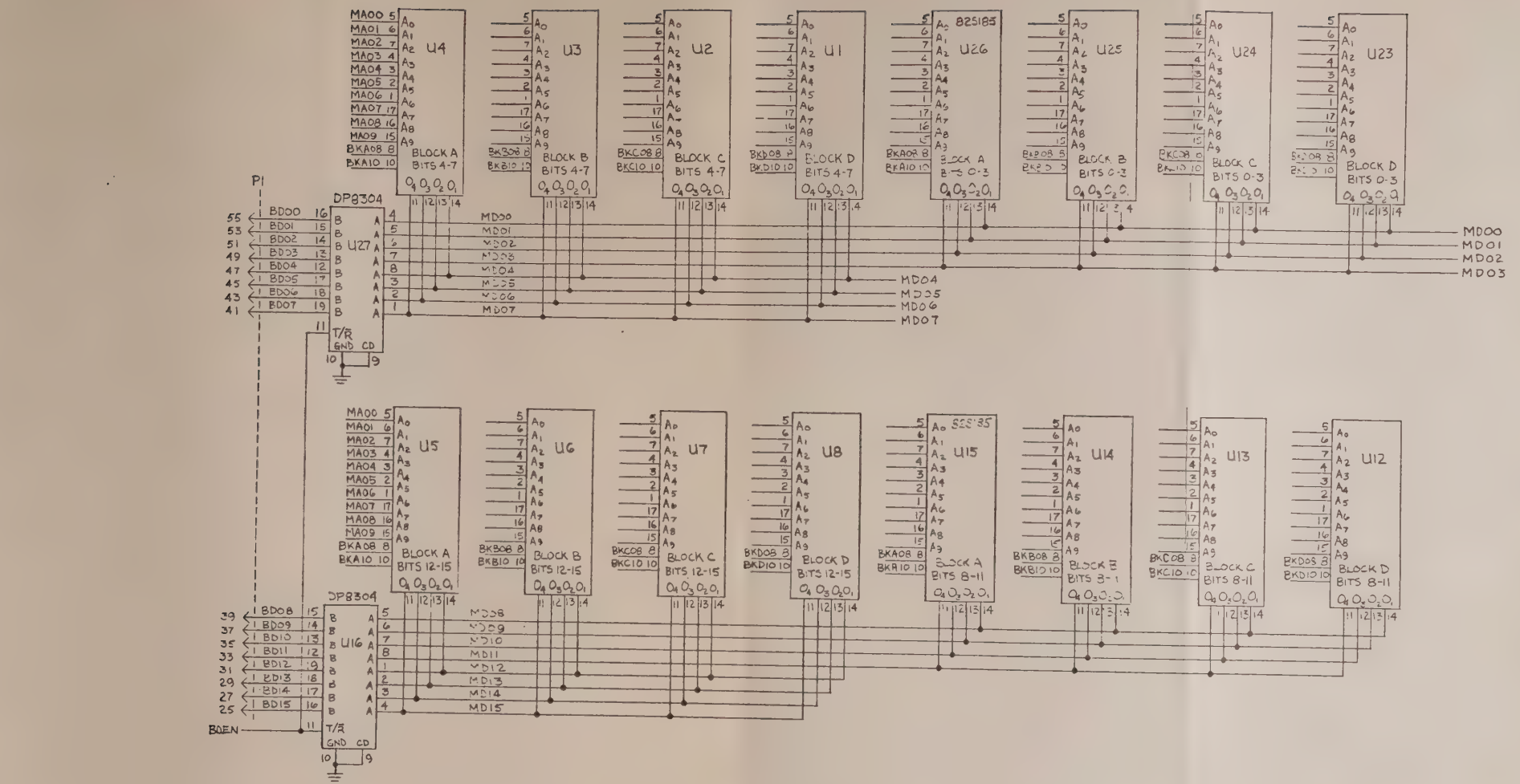
8 (-1) SPRAY CONFORMAL COAT BOTH SIDES
7 (-2) FOR MODEL 9642. DELETE ITEMS IN TABULATION
6 INSTALL ITEM 141 (EJECTOR) WITH ITEM 142 (EYELET) AND SWAGE IN PLACE
5 (-3) IS FOR GENERAL USE REQUIRING CURRENT LIMITING RESISTORS.
4 (-1) IS FOR 9007/9629 RANGE SIMULATOR.
3. REF TO PL190-237-4 FOR PARTS LIST
2. ALL CAPS IN μfd
1. ALL RESISTORS IN OHMS ¼W 5%
NOTES: UNLESS OTHERWISE SPECIFIED

TABULATION BLOCK	
DASH NO.	DESCRIPTION
-1	USE JUMPERS FOR R18-R25
-3	USE SELECTED RESISTORS
-2	DELETE C4-C11, R18-R25, U7, U16, U19, U28, U29

ITS-1190103-60-E

SHT 1 OF 1

Figure 5-6
Front Panel Controller Card
1A8A3, Assembly Drawing



5 -1 AND -2 VERSIONS ONLY

4 DO NOT ASSIGN THE SAME BLOCK NO. TO ROM & RAM

3 USE 2 JUMPERS TO SELECT EACH BLOCK OF ROM OR RAM

2. ALL CAPACITORS IN MICROFARADS

1. ALL RESISTORS ¼W. ±5%

NOTES: UNLESS OTHERWISE SPECIFIED

9. ROM IC's - 825185 (2K × 4 BITS)

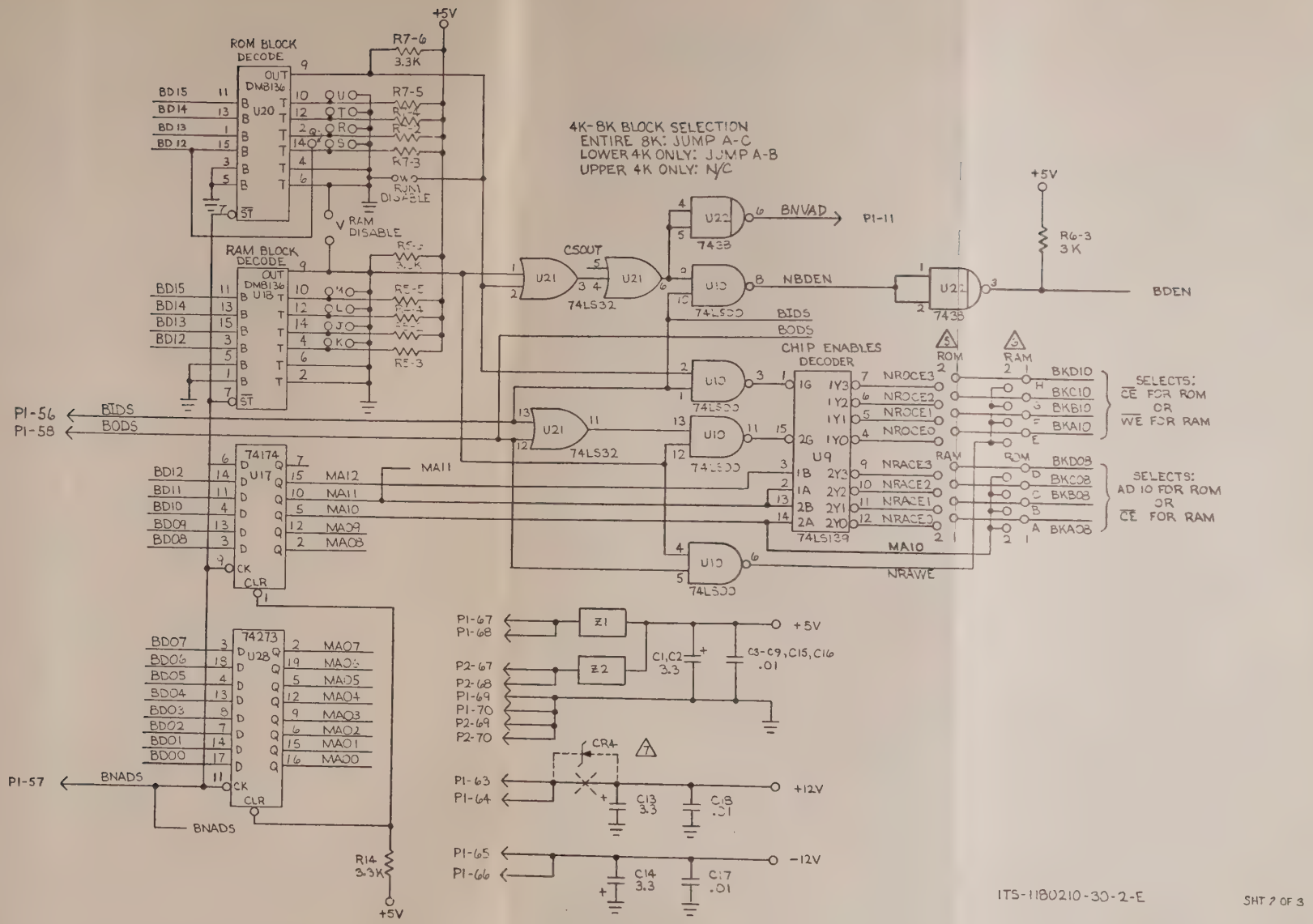
8. RAM IC's - 2114 (1K × 4 BITS)

7. CARD ACCOMODATES 4 BLOCKS OF MEMORY, DESIGNATED A, B, C, AND D

6. ALL IC'S IN ONE BLOCK MUST BE SAME TYPE

ITS-1180210-30-1-E SHT 1 OF 3

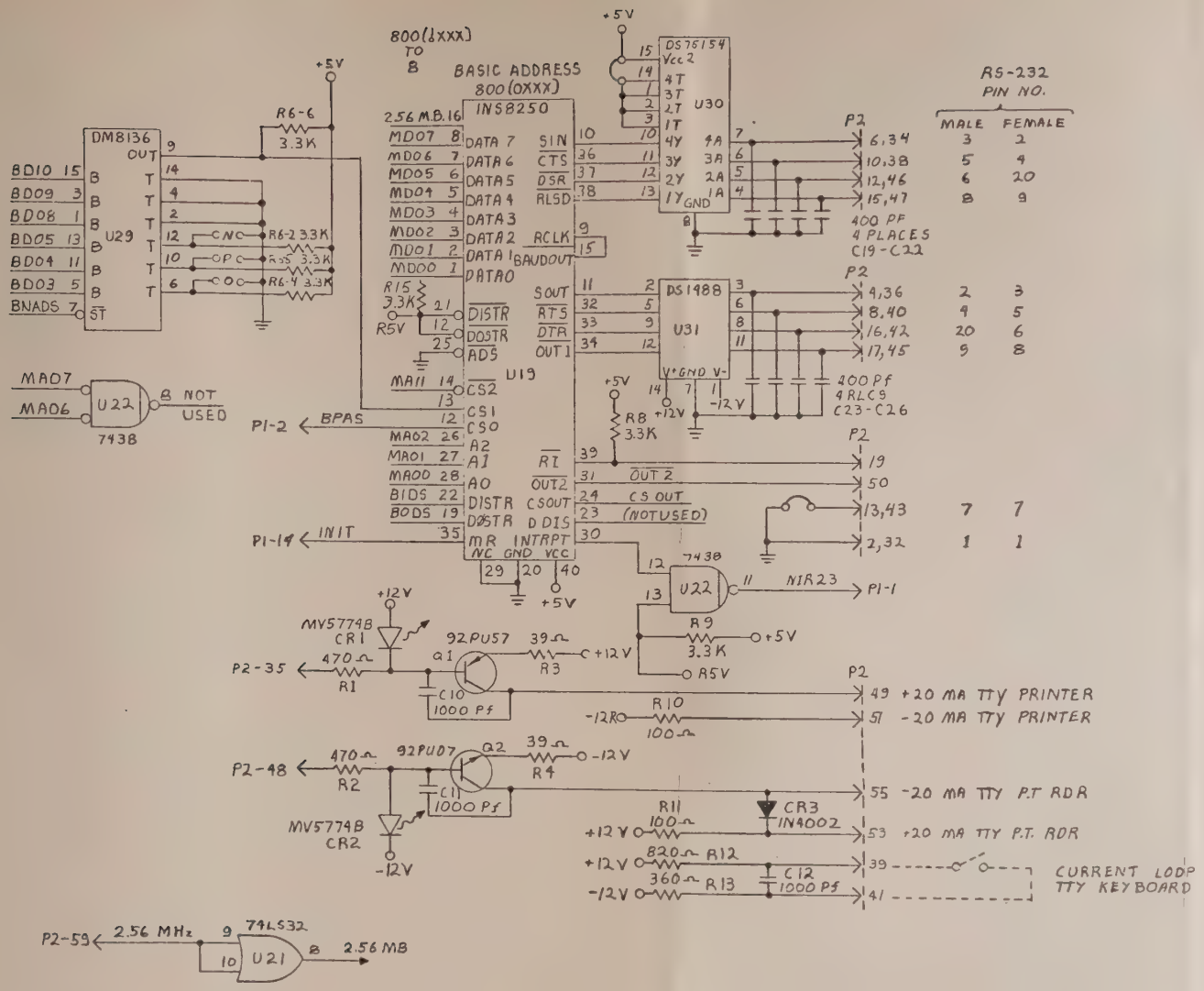
Figure 5-7
RAM/ROM RS-232 Card
1A9A4, Schematic Diagram



ITS-1180210-30-2-E

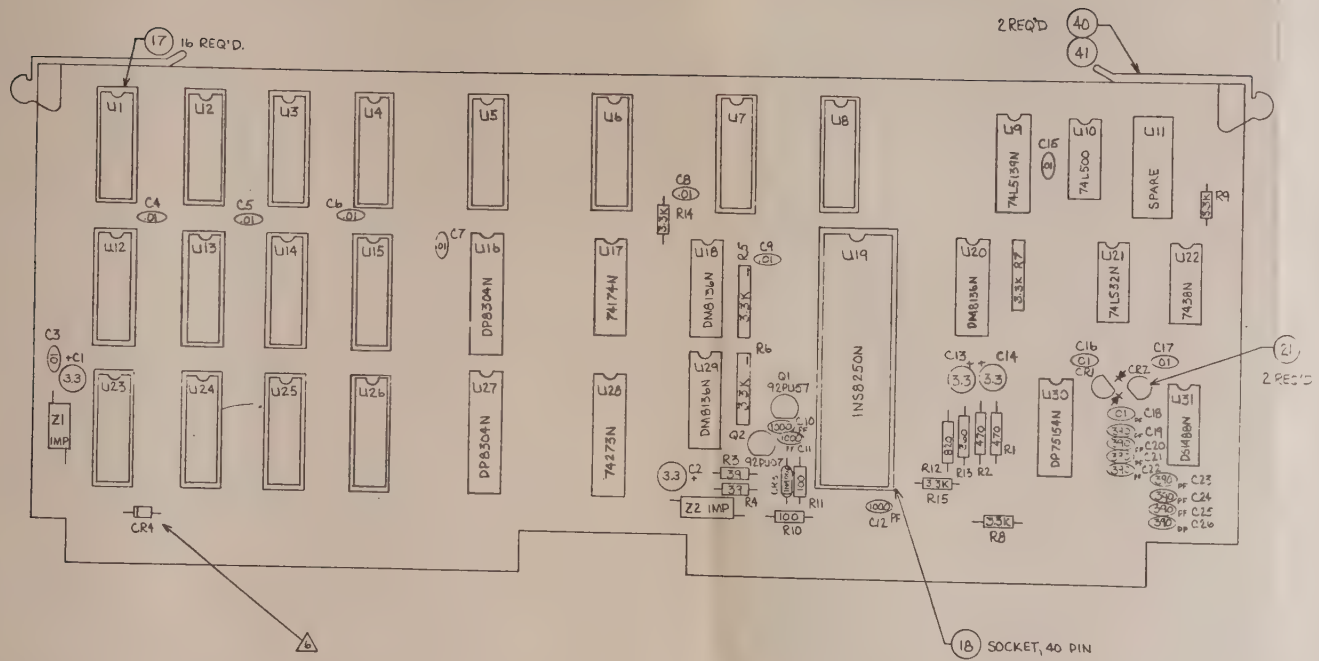
SHT 7 OF 3

Figure 5-7
RAM/ROM RS-232 Card
1A9A4, Schematic Diagram



ITS-11R0210-30-3-E SHT 3 OF 3

Figure 5-7
RAM/ROM RS-232 Card
1A9A4, Schematic Diagram



⚠6 -1, -2 ONLY INSERT CR4, CUT TRACE BETWEEN LEADS (CKT SIDE)
⚠INSTALL JUMPERS PER DASH NUMBER (PAGE 2) TABULATION
⚠INSTALL ITEM 40 (EJECTOR) WITH ITEM 41 (EYELET) AND SWAGE IN PLACE
3. FOR P/L SEE 1140210-10
2. CAPACITORS ARE IN MFDS
1. RESISTORS ARE IN OHMS, ¼W, 5%
NOTES: UNLESS OTHERWISE SPECIFIED

ITS-1180210-60-1-E

SHT 1 OF 2

Figure 5-8
RAM/ROM RS-232 Card
1A9A4, Assembly Drawing

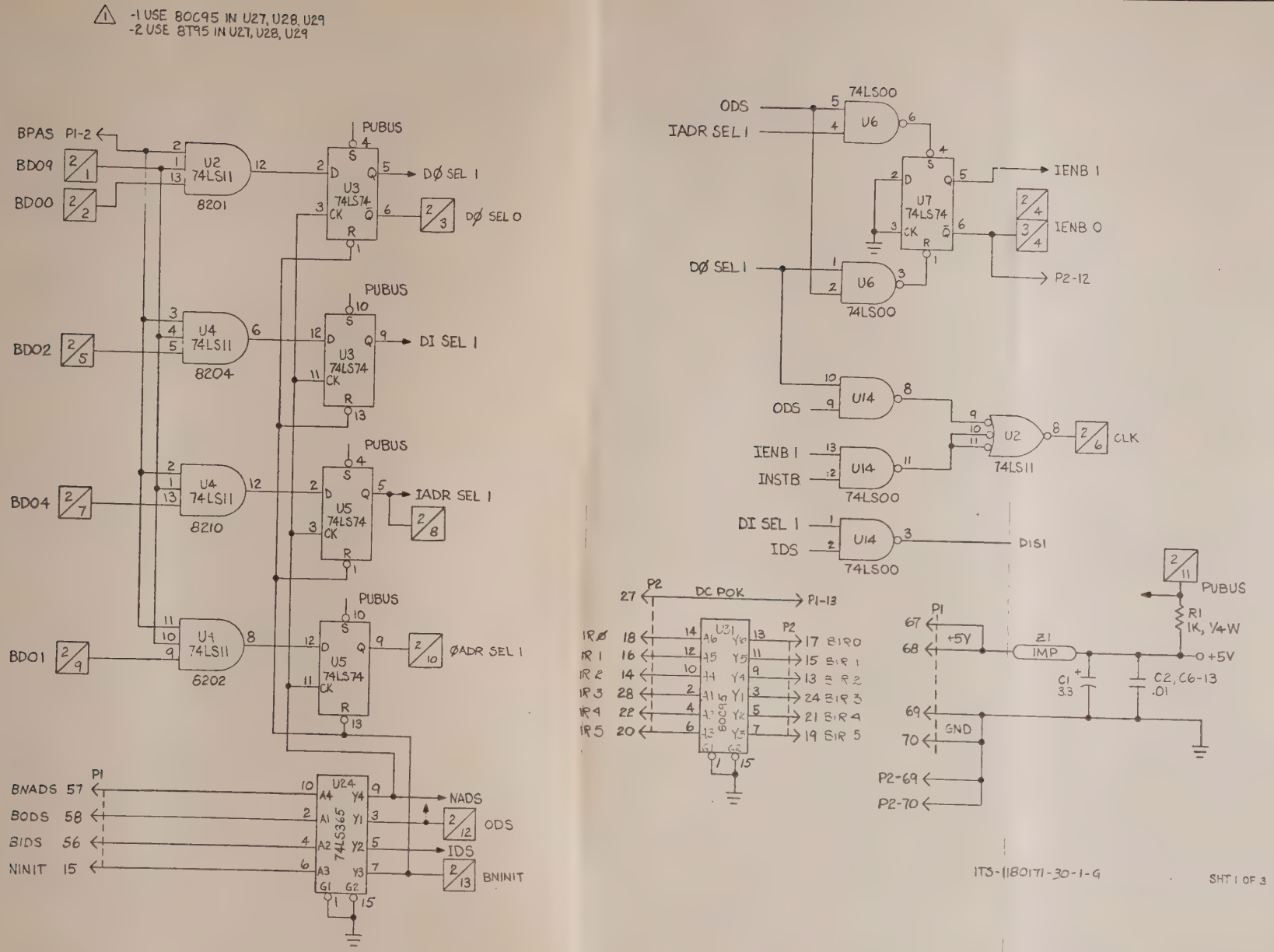
TABULATION PARTS		
DASH NO.	ROM-825185	RAM-2114
-1	U3, 4, 5, 6, 14, 25, 26	—
(-1 CONT.)	U7, 13, 15, 24, 2	—
(-1 CONT.)	INSTALL CR4	
-2	—	U1, U12, U23, U8
(-2 CONT.)	INSTALL CR4	

TABULATION JUMPERS																		
DASH NO.	ROM 1 TO ROM 2	RAM 1 TO RAM 2	J	K	L	M	N	O	P	Q	R	S	T	U	V	W
-1	A — A	G — A		X	X	X	X	X	X		X		X	X	X	
	B — B															
	C — C															
	E — G															
	F — H															
-2		A — A					X	X	X							X
		B — B														
		C — C														
		D — D														
		E — E														
		F — F														
		G — G														
		H — H														

X = JUMPER INSTALLED

ITS-1180210-GO-2-E

Figure 5-8
RAM/ROM RS-232 Card
1A9A4, Assembly Drawing



ITS-1180171-30-1-G

SHT 1 OF 3

Figure 5-9
Command/Data Card
1A9A5, Schematic Diagram

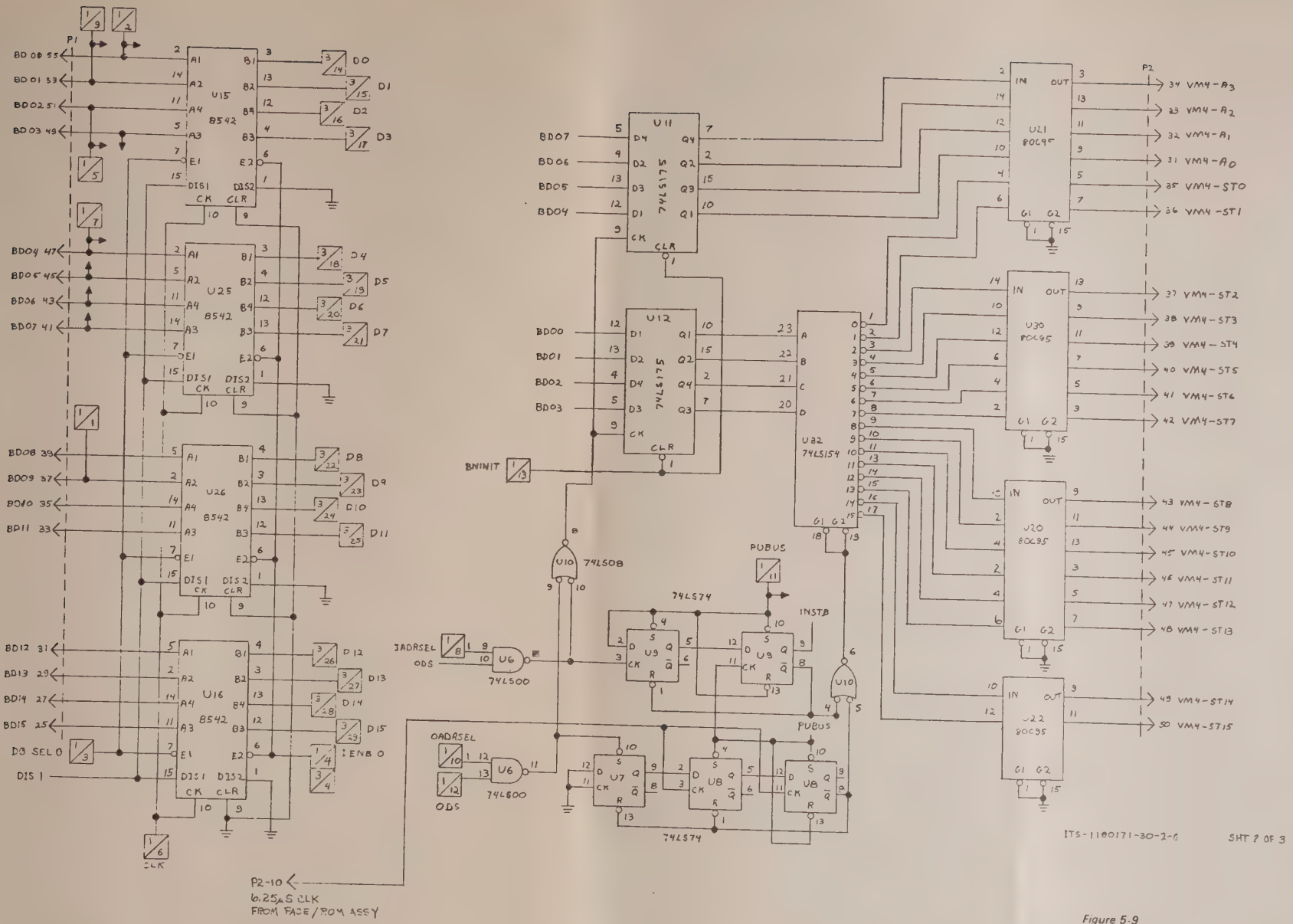


Figure 5-9
Command/Data Card
1A9A5, Schematic Diagram

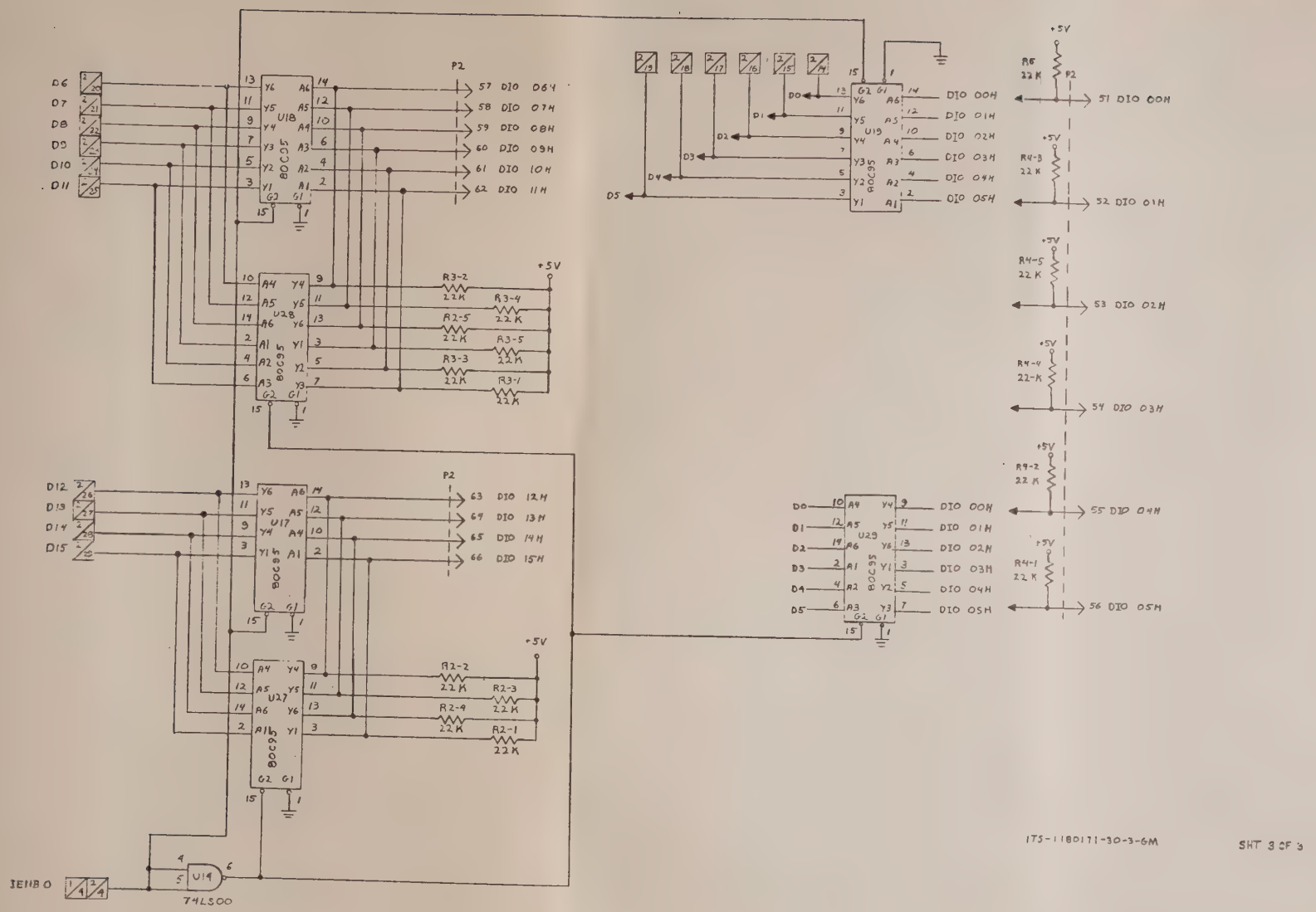
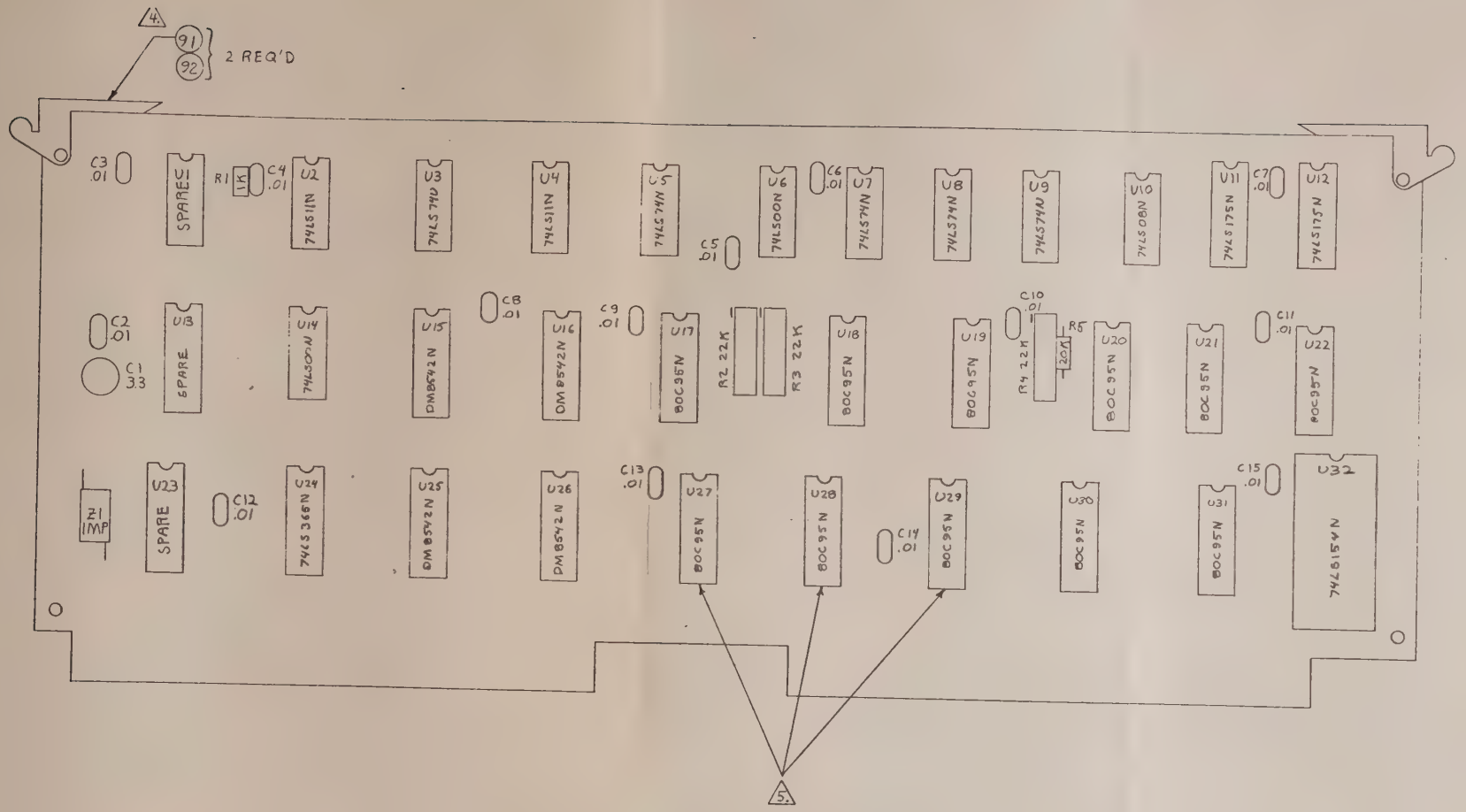


Figure 5-9
Command/Data Card
1A9A5, Schematic Diagram



ITS-1180171-60-E

SHT 1 OF 1

4 -2 ONLY: CHANGE I.C. TO 8T95

4 INSTALL ITEM 91 (EJECTOR) WITH ITEM 92 (EYELET) & SWAGE IN PLACE

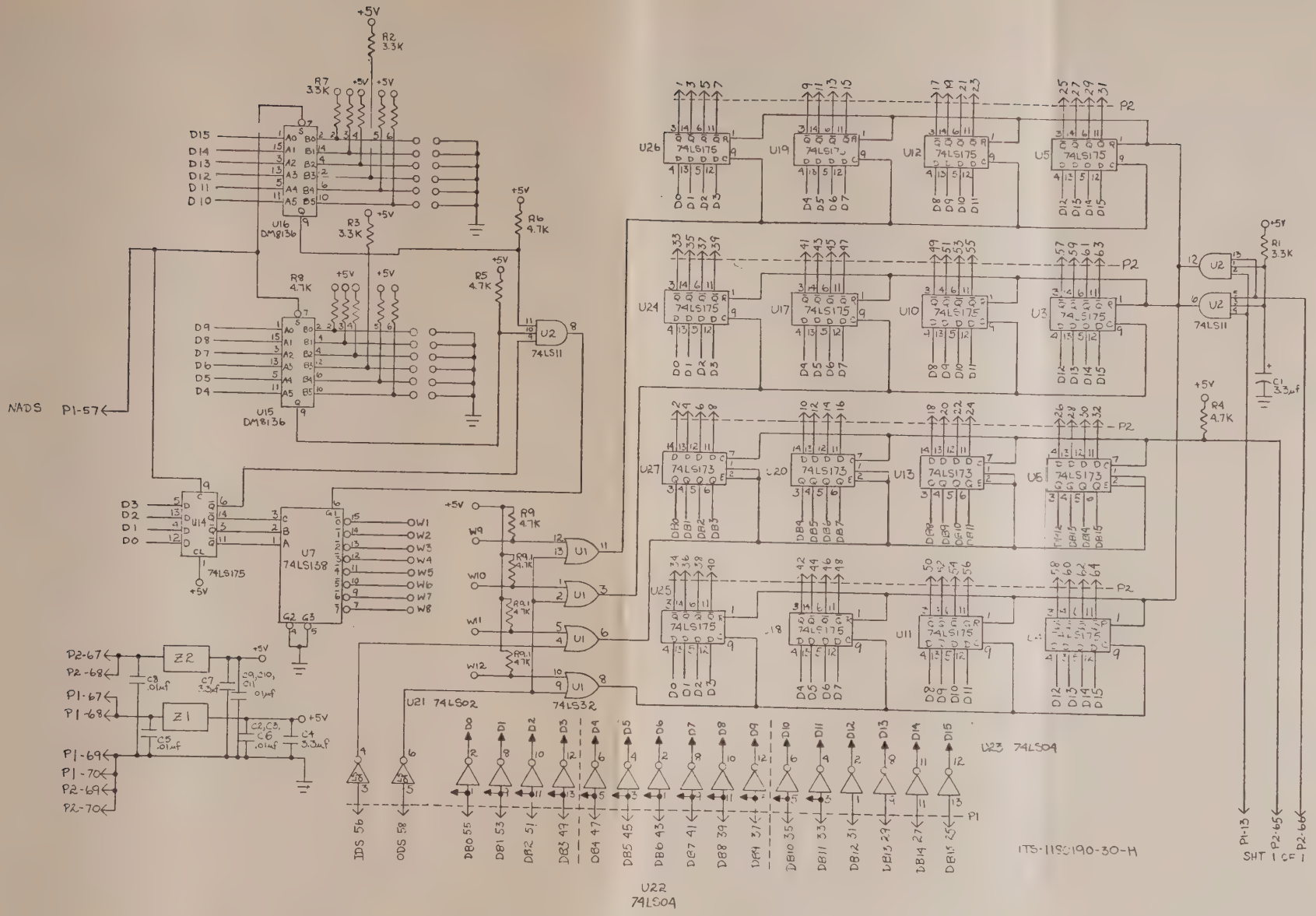
3. FOR P/L SEE PL190-287-6

2. CAPACITORS ARE IN MICROFARADS

1. RESISTORS IN OHMS, ¼ W, 5%

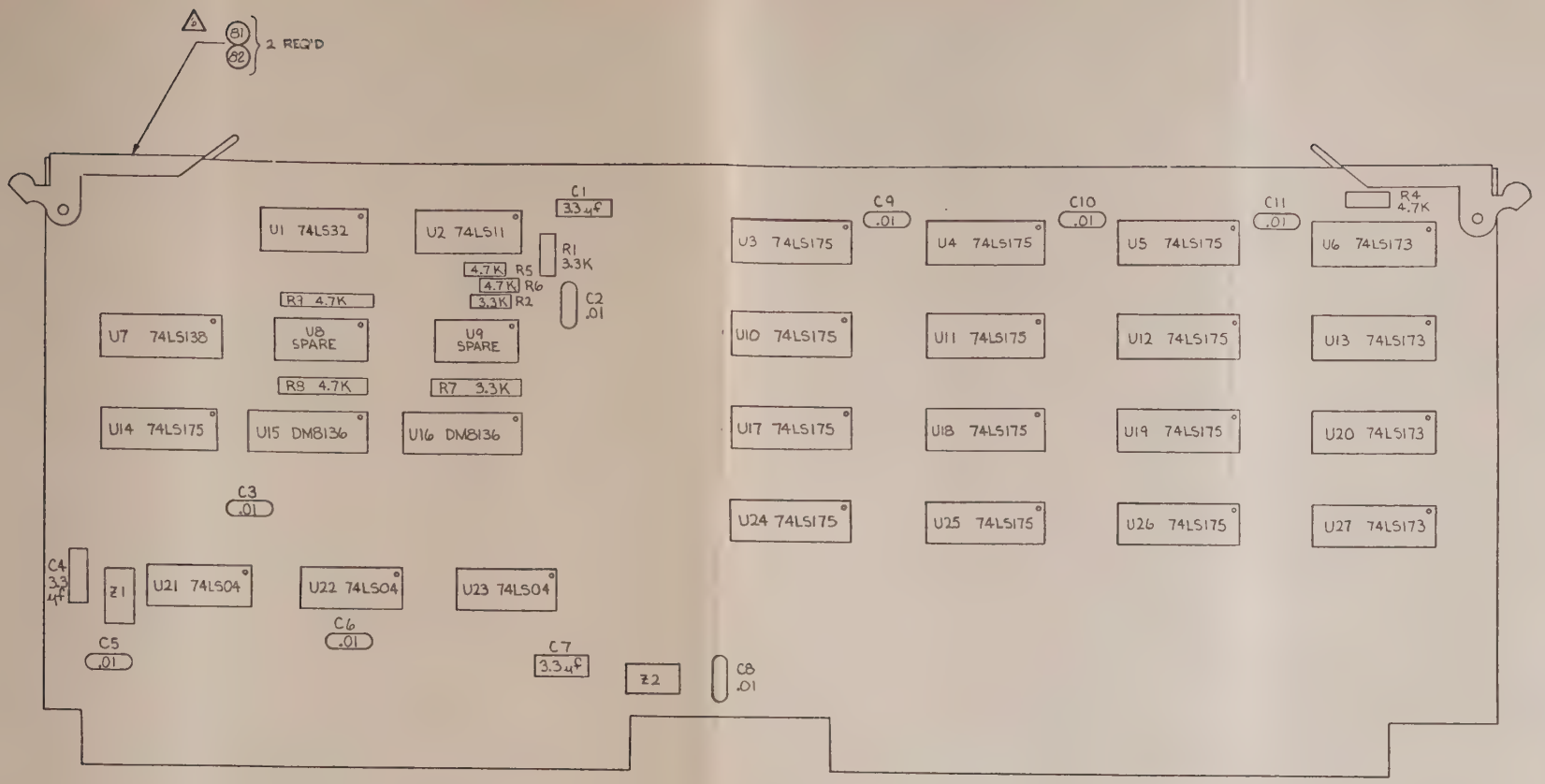
NOTES: UNLESS OTHERWISE SPECIFIED

Figure 5-10
Command/Data Card
1A9A5, Assembly Drawing



3. DO NOT INSTALL R3 FOR -2 CONFIGURATION
2. SEE C190-287-7 FOR DASH NO. TABULATIONS.
1. DEVICE ADDRESS JUMPERS ARE FACTORY SET.
NOTES: UNLESS OTHERWISE SPECIFIED.

Figure 5-11
L.E.D. Parallel I/O Card
1A9A7, Schematic Diagram



TABULATION
-1 CONFIGURATION- JUMPER THE FOLLOWING POINTS: W1 TO W9, W4 TO W12, W6 TO W11, U9-1 TO U9-12, W7 TO W10
-2 CONFIGURATION- A. OMIT U5, U12, U19 & U26 (74LS175) B. IN PLACE OF 74LS175'S SUBSTITUTE 74175'S (8 PLACES) EXCEPT U14 C. JUMPER THE FOLLOWING POINTS: W5 TO W10, W6 TO W12, W8-W11, U9-1 TO U9-12, U9-5 TO U9-8

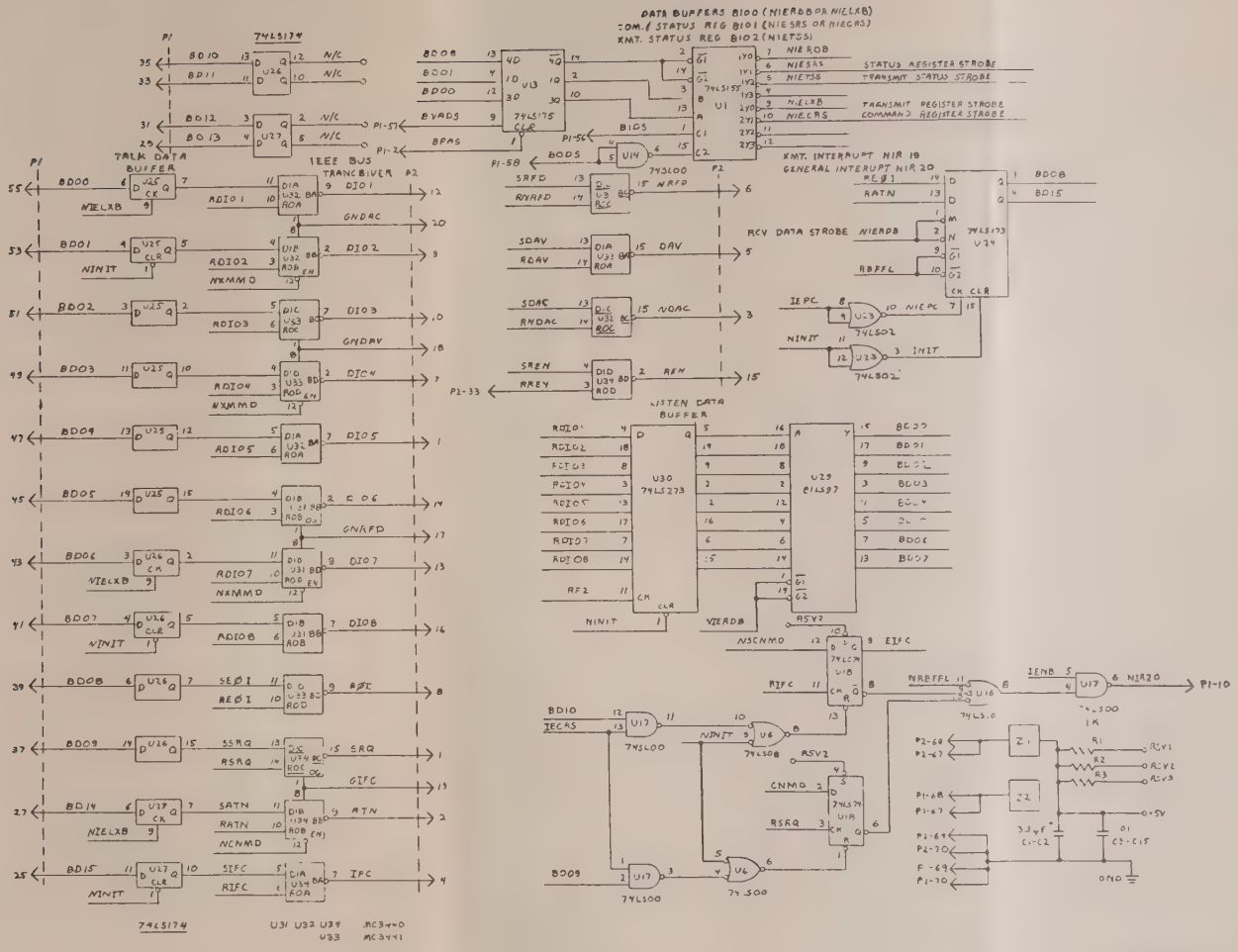
7. -1 BOARD SPRAY CONFORMAL COAT BOTH SIDES
6. INSTALL ITEM 81 (EJECTOR) WITH ITEM 82 (EYELET) AND SWAGE IN PLACE
5. FOR DWG. DASH NO. SEE TABULATION BLOCK
4. DEVICE ADDRESS JUMPERS ARE FACTORY SET
3. FOR PARTS LIST SEE PL190-287-7
2. CAPACITORS ARE IN MICROFARADS
1. RESISTORS ARE IN OHMS 5%, 1/4W

NOTES: ULESS OTHERWISE SPECIFIED

ITS-1180190-60-L

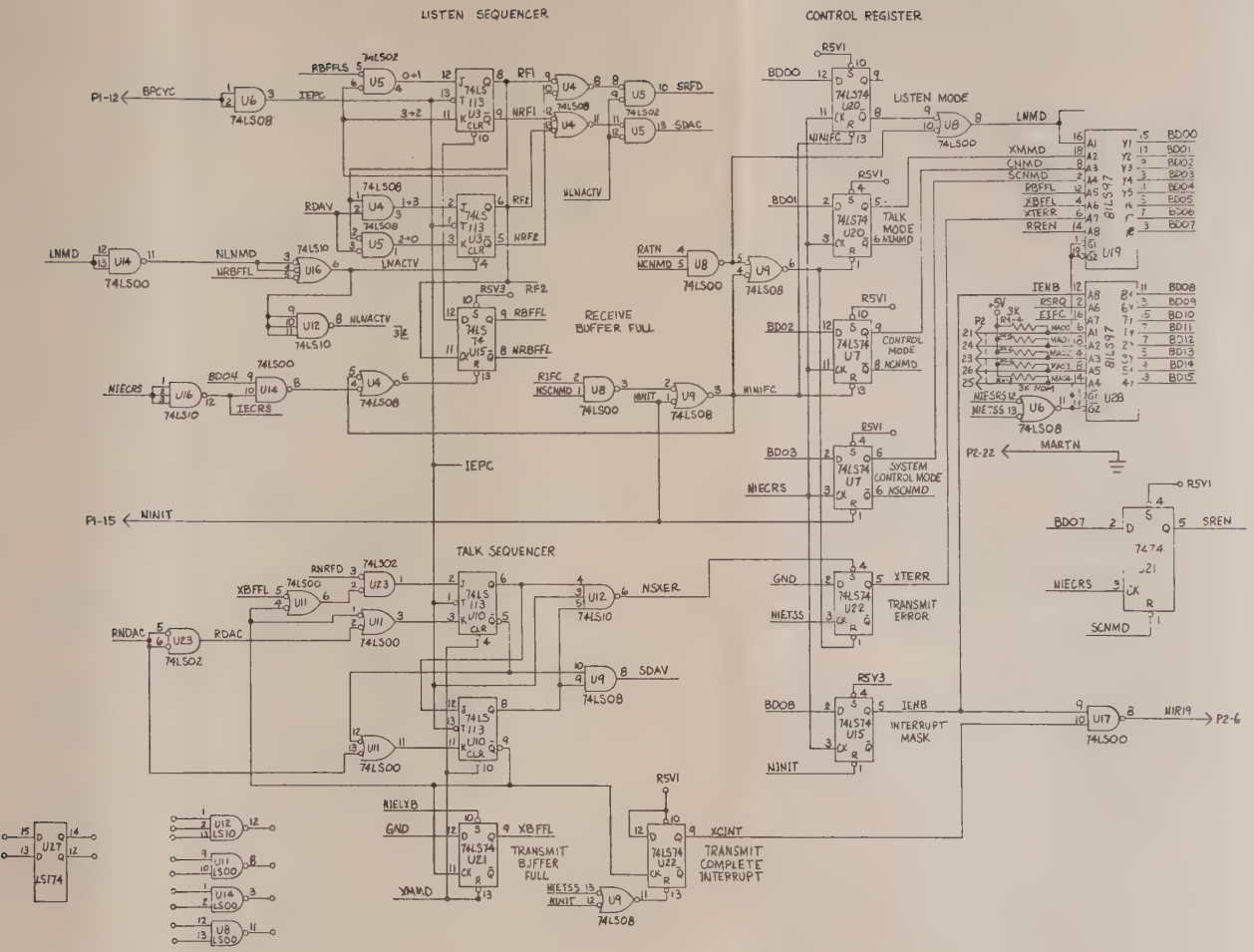
SHT 1 OF 1

Figure 5-12
L.E.D. Parallel I/O Card
1A9A7, Assembly Drawing



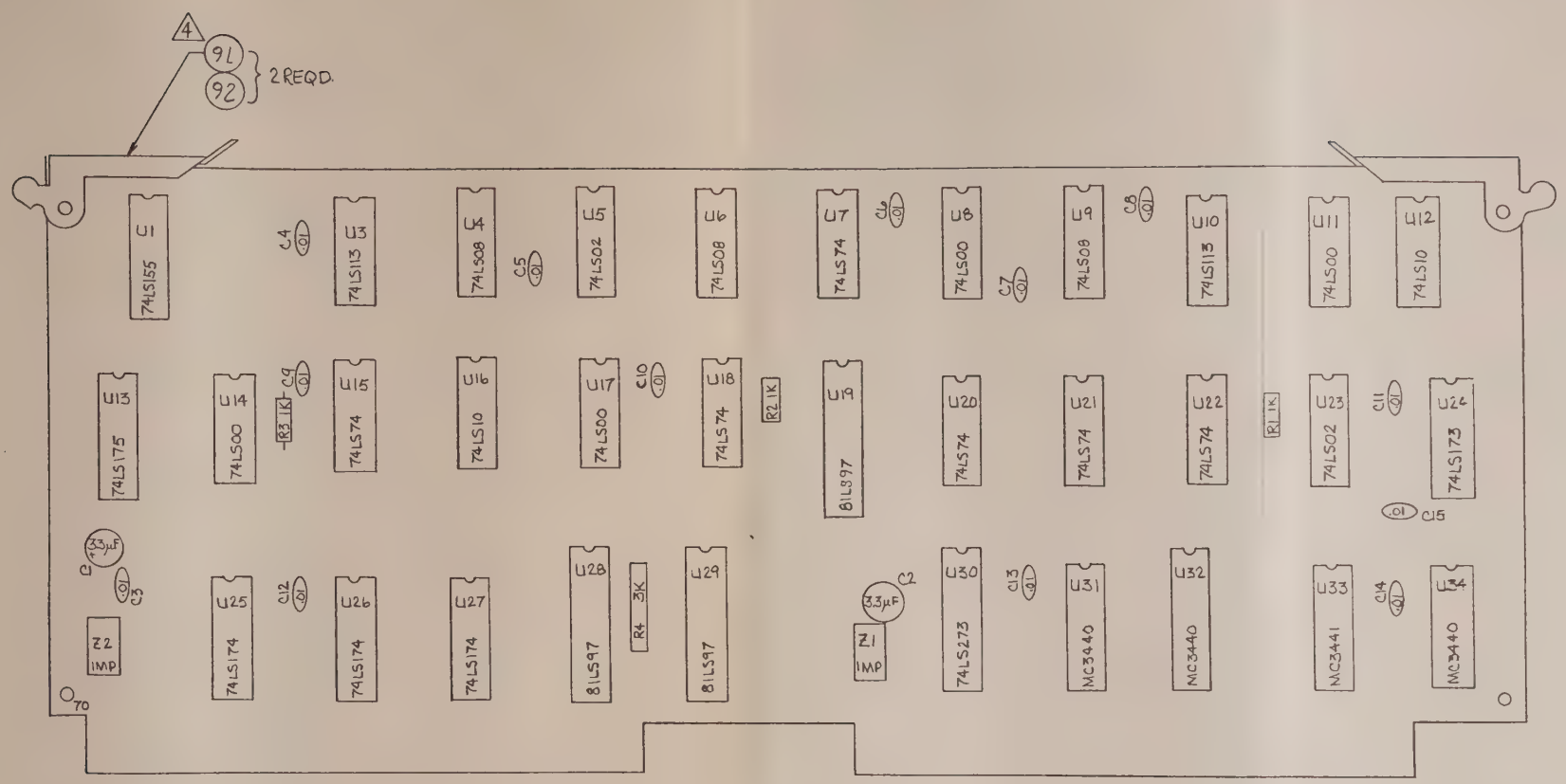
2 ALL RESISTORS IN OHMS ¼W 5%
1 ALL CAPS IN MFD
NOTES: UNLESS OTHERWISE SPECIFIED

Figure 5-13
IEEE Interface Card
1A9A8, Schematic Diagram



1T5-1180141-30-2-D SHT 2 OF 2

Figure 5-13
IEEE Interface Card
1A9A8, Schematic Diagram

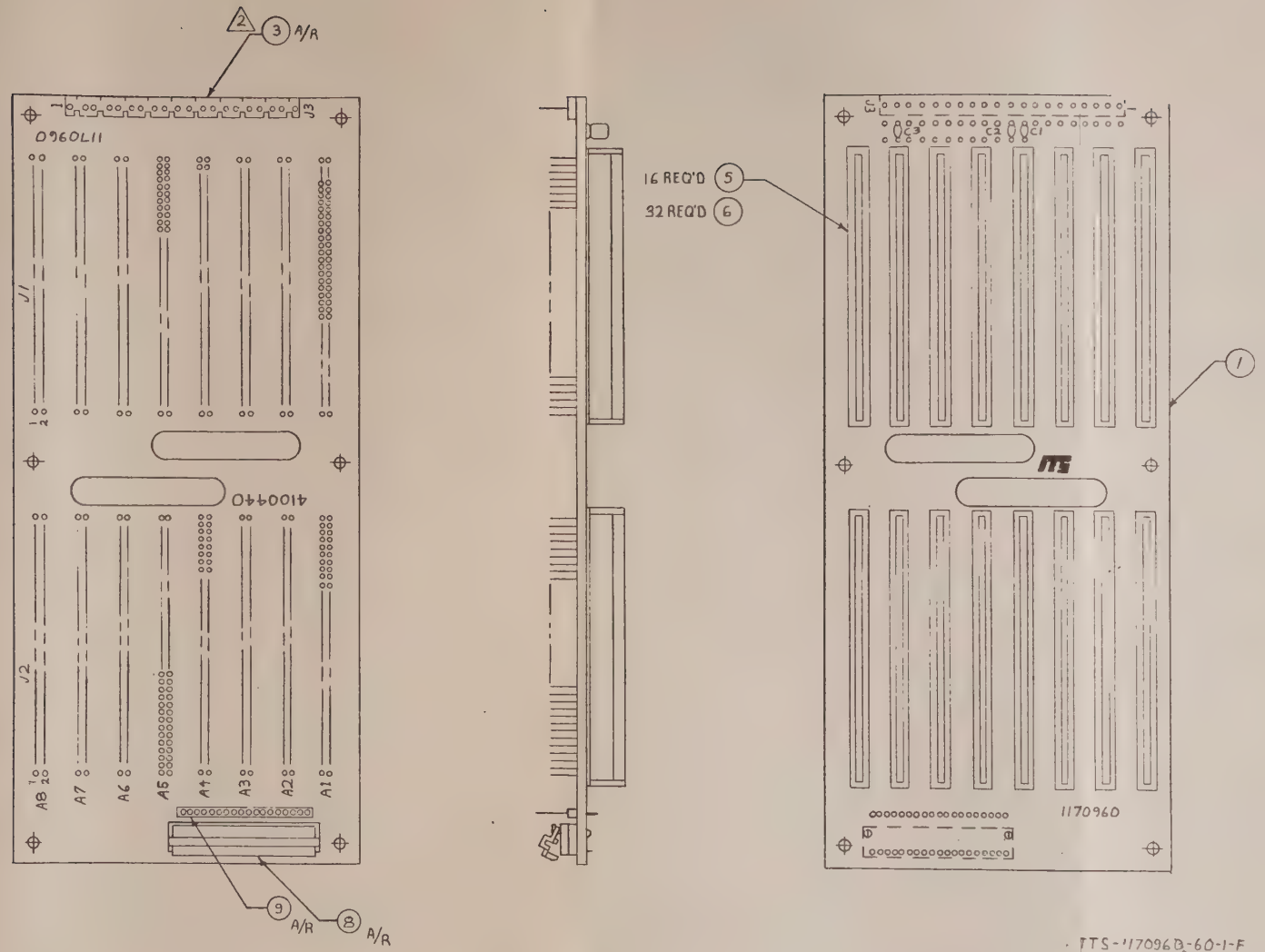


ITS-1180141-60-F

SHT 1 OF 1

5. 9629 SPRAY CONFORMAL COAT BOTH SIDES
4. INSTALL ITEM 91 (EJECTOR) WITH ITEM 92 (EYELET) AND, SWAGE IN PLACE
3. REF TO FL190-2878 FOR PARTS LIST
2. ALL RESISTORS IN OHMS ¼ W, 5%
1. ALL CAPACITORS IN MICROFARADS
NOTES: UNLESS OTHERWISE SPECIFIED

Figure 5-14
IEEE Interface Card
1A9A8, Assembly Drawing



FTS-117096D-60-1-F SHT 1 OF 2

4. THIS DRAWING IS OF DASH 1. SEE TABULATION FOR APPROPRIATE DEVIATIONS AND JUMPERS
3. ALL CAPACITORS 0.1μF, ±20%, 100V
2. INDEXED COMPONENT. DASH 1 SHOWN. DASH 2 INSTALL ON TOP
1. SEE PL 190-287-1 FOR PARTS LIST.
NOTES: UNLESS OTHERWISE SPECIFIED

Figure 5-15
PACE Subsystem
Motherboard
Assembly Drawing

TABULATION											
DASH NO.	COMPONENTS										
-1	JUMPER A1J1-37TO A1J1-38	JUMPER A1J1-40TO A1J1-49	JUMPER A1J2-59TO A5J2-10	JUMPER A1J2-55TO A4J2-59	JUMPER A5J2-24TO A5J1-60	JUMPER A7J2-65 A7J1-56					
	JUMPER J4-1 A3J2-45	JUMPER J4-2 A3J2-45	JUMPER J4-3 A3J2-49	JUMPER J4-4 A3J2-50	JUMPER J4-5 A3J2-30	JUMPER J4-6 A3J2-31	JUMPER J4-7 A3J2-33	JUMPER J4-8 A3J2-29	JUMPER J4-9 A3J2-32	JUMPER J4-10 A3J2-34	
	J4-11 BLANK	JUMPER J4-12 A3J2-35	JUMPER J4-13 A3J2-37	JUMPER J4-14 A3J2-48	JUMPER J4-15 A3J2-51	JUMPER J4-16 A3J2-52	JUMPER J4-17 A3J2-43	JUMPER J4-18 A3J2-44			
-2	A1J1-32TO A1J1-38	A1J1-42TO A1J1-44	A1J1-26TO A6J2-23	A6J2- A7J2-	1-3-5-7-9 1-3-5-7-9	11-13-15-17 11-13-15-17	19-21-23-25 19-21-23-25	27-29-31 27-29-31	A6J2-2TO A7J2-33	A6J2-4TO A7J2-35	
	A6J2-6TO A7J2-37	A6J2-8TO A7J2-39	A6J2-18TO A7J2-49	A6J2-20TO A7J2-51	A6J2-22TO A7J2-53	A6J2-24TO A7J2-55		A6J1-63,64 TO A6J2-65,66 24GAWIRE			
	DELETE ITEMS ⑤ & ⑨		CUT PINS A8J2-27,28 A3J2-27,	28,29,30,66							
-3	A1J1-32TO A1J1-38	A1J1-40 TO A1J1-44	A1J2-55 TO A4J2-59	A1J2-59 TO A5J2-10	A7J2-65TO A7J1-56	DELETE ITEMS ②,③,④					

ITS-1170960-60-2-F SHT 2 OF 2

Figure 5-15
PACE Subsystem
Motherboard
Assembly Drawing

MP MASTER
MA35912